800 W Platinum® server power supply

Using 600 V CoolMOS™ C7 and digital control with XMC™

About this document

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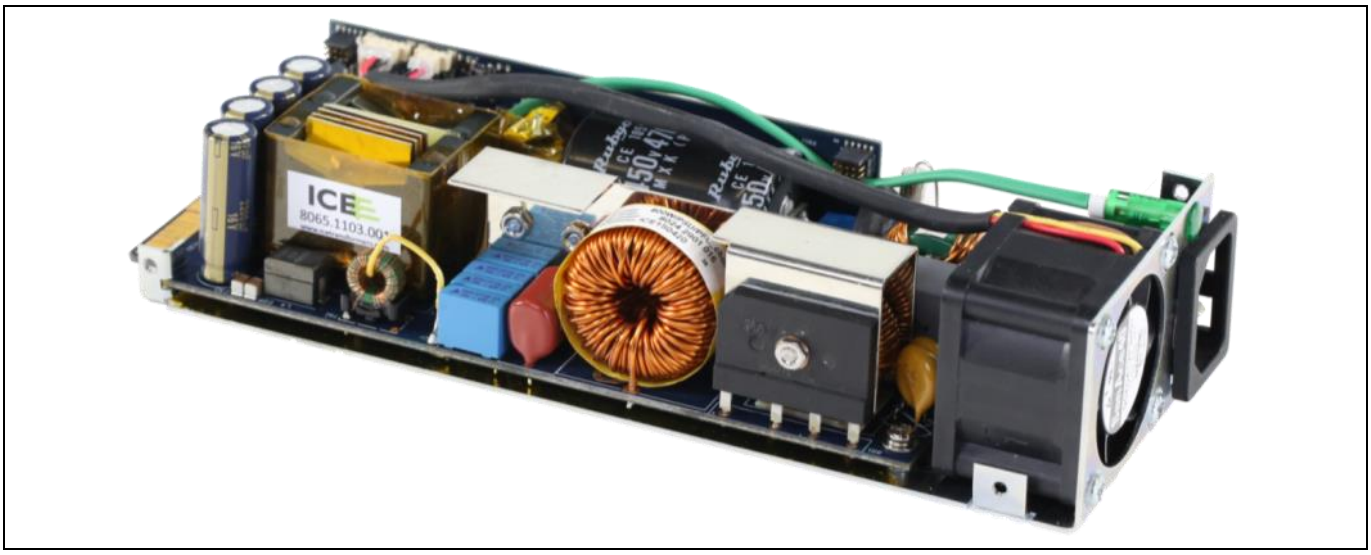
Scope and purpose

This document introduces a complete Infineon system solution for an 800 W server power supply, which achieves the 80Plus® Platinum® standard. The power supply is composed of a Continuous Conduction Mode (CCM) Power Factor Correction (PFC) converter and a half-bridge LLC DC-DC converter. This document focuses on the necessary microcontroller configuration and the implemented control for adequate system performance, which is demonstrated with test results.

The Infineon components used in the 800 W server power supply are:

- 600 V CoolMOS™ C7 superjunction MOSFET in TO-247 4-pin and TO-220 packages as well as 650 V CoolSiC™ Schottky diode Gen5
- 40 V and 25 V OptiMOS™ 5 MOSFETs
- 1EDI20N12AF isolated and 2EDN7524F non-isolated gate drivers (EiceDRIVER™)
- XMC1402 and XMC4200 microcontrollers
- ICE2QR2280G CoolSET™ QR flyback controller



Intended audience

This document is intended for design engineers who want to verify the performance of:

- The 600 V CoolMOS™ C7 MOSFET technology in TO-247 4-pin package in hard-switching topologies like the CCM PFC boost converter working at 65 kHz along with the 650 V CoolSiC™ Schottky diode Gen5

Summary of the 800 W Platinum® server power supply

- The 600 V CoolMOS™ C7 MOSFET technology in soft-switching topologies like the LLC working at a resonant frequency around 150 kHz
- The isolated and the non-isolated gate drivers from the EiceDRIVER™ IC family
- The flexibility and performance power of the XMC™ microcontrollers for server power supplies

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1 Summary of the 800 W Platinum® server power supply

This Application Note provides a very detailed description of the design considerations and operation under both steady-state and abnormal operating conditions, as well as results of a total Platinum® efficiency compliant server power supply, by using several different Infineon Technologies semiconductors, ranging from power MOSFETs to microcontrollers.

Below is a summary of the key features that this demo board offers when used as a reference for power supplies in server applications:

- Attractive compact design in 30 W/in^3 form factor
- Efficiency that outperforms the Platinum® efficiency standard throughout the entire load demand at both 115 V AC and 230 V AC, as shown in Performance and steady-state operation Figure 41 in section 6.1
- Low Total Harmonic Distortion (THD) and high PF response, as shown in Figure 42 and Figure 43 respectively, from 20% of the load
- Fully digital control implementation in both the PFC boost converter using XMC1400, as described in the Power factor correction stage section, and the LLC resonant converter using the XMC4200, as described in the LLC resonant DC-DC converter section
- High performance achieved by using Infineon Technologies best-in-class devices:
    - Single TO-247 4-pin 600 V CoolMOS™ C7 SJ MOSFET in the PFC boost converter, along with a single TO-220 650 V CoolSiC™ schottky diode Gen5
    - TO-220 600 V CoolMOS™ C7 SJ MOSFET on the primary side of the LLC resonant converter and OptiMOS™ 5 40 V and 25 V as Synchronous Rectification (SR) and ORing MOSFETs, respectively
    - EiceDRIVER™ 1EDI isolated and EiceDRIVER™ 2EDN non-isolated gate driver ICs
    - QR flyback controller ICE2QR2280G CoolSET™
- Robust and realiable operation under different abnormal conditions:
    - Smooth inrush current during start-up as shown in Figure 46
    - Power Line Disturbance (PLD) events, like AC Line Drop Out (ACLDO) as described in Table 8, as well as voltage sags as describes in Table 9
    - Brownout reaction as shown in Figure 58
    - Load-step reponse at different abrupt load changes as shown in Figure 59 and Figure 60
    - Over Current (OC) condition reaction as described in the Over Current Protection (OCP) section, as well as the response of the PSU in case of a short-circuit event, as shown in Figure 65
- Fully compliant with both peak and average Class B conducted EMI EN 55022 standard limits, as shown in Figure 66 and Figure 67

2 System description

This document presents an Infineon system solution for an 800 W server power supply in 30 W/in^3. The evaluation board consists of a classic CCM PFC boost converter with average current control at AC-DC stage. The PFC converter provides regulated bulk voltage from a universal AC input, while it demands high-quality current from the grid. The DC-DC stage is an LLC resonant converter, which provides 12 V regulated output. Both converters have a dedicated Infineon microcontroller to manage the converter control as well as the system behavior.

Figure 1 shows a block diagram of the implemented power supply with the blocks as described. In addition, an ORing switch is implemented in anticipation of the efficiency of a full system solution, even though no advance ORing functionality is implemented. Furthermore, an I_2C channel is reserved in the secondary controller, which enables PMBus communication implementation.

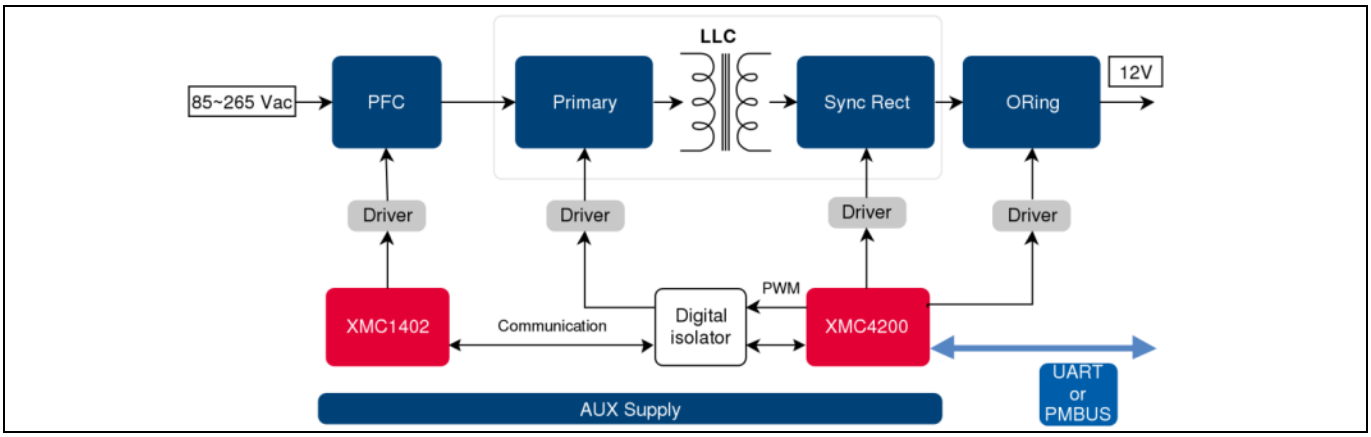

Figure 1 800 W server power supply block diagram

The target level of the 800 W server power supply is Platinum® efficiency according to the 80Plus® standard. As shown in Figure 2, this efficiency level is reached with a wide margin, which makes the obtained efficiency close to Titanium® level for light and full-load.

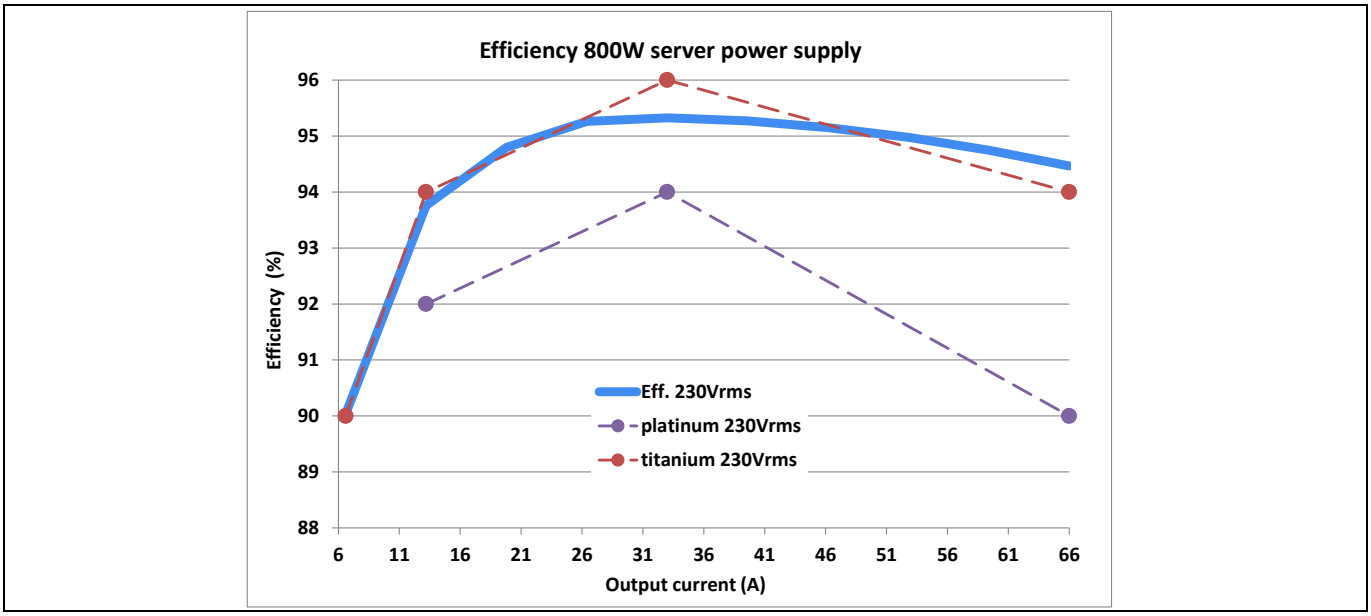

Figure 2 Measured efficiency of the 800 W server power supply compared to the Platinum® and Titanium® standards

2.1 Specifications

This section describes the main electrical specifications of the Infineon server power supply evaluation board for both input and output.

The requirements for the universal AC input are introduced in Table 1, as well the required hold-up times to provide regulated output when the AC input is not present.

Table 1 Input requirements

Parameter	Value
Input voltage range, V_{in_range}	90–265 V AC
Nominal input voltage, V_{in}	230 V AC
AC-line frequency range, F_{AC}	47–63 Hz
Max peak input current, I_{in_max}	10 A_{RMS} @ V_{in} = 90 V AC, P_{out_max} = 800 W
Turn-on input voltage, V_{in_on}	80–87 V AC, ramping up
Turn-off input voltage, V_{in_off}	75–85 V AC, ramping down
PFC, PF	Shall be greater than 0.9 from 20% rated load and above
Hold-up times	10 ms after last AC zero point @ P_{out_max} 20 ms after last AC zero point @ 0.5 × P_{out_max}
THD	< 10% from 20% load @ high-line, for class A equipment

In the case of the regulated 12 V output, the requirements are shown in Table 2. It should be mentioned that the output voltage dynamic range considered must be maintain not only in dynamic load conditions, but also in case of PLD of the AC input.

Table 2 Output requirements

Parameter	Value
Nominal output voltage	12.2 V ± 2% in static conditions at nominal V_{in}
Nominal output current	67 A
Output voltage ripple	Max 120 mVpk-pk at I_{out} = 67 A
Output OV set point	Min 13.5 V max 14 V
Output OC threshold	30 s up to 74 A 10 s up to 83 A Max 1 ms over 83 A
Dynamic output voltage variation	±240 mV *Note: Load-step 3–33 A and 33–66 A with 0.5 A/µs current slope* *Note: Input voltage variation and PLD*

Table 3 Overal efficiency target

Load condition	Efficiency @ low-line	Efficiency @ high-line
20%	90%	90%
50%	92%	94%
100%	90%	91%

2.2 Infineon Technologies semiconductors

2.2.1 600 V CoolMOS™ C7

The 600 V CoolMOS™ C7 series of devices offers a ~50% reduction in turn-off losses compared to the CoolMOS™ CP, offering a GaN-like level of performance in PFC, TTF and other hard-switching topologies. The CoolMOS™ C7 delivers an area-specific on-resistance ($R_{DS(ON)}$*A) of just 1Ω per mm^2, extending Infineon's portfolio of products with lowest $R_{DS(ON)}$ per package to support customer efforts to further increase power density.

The 600 V CoolMOS C7 series features ultra-low switching losses and targets high-power SMPS applications such as server, telecom, solar and industrial applications requiring high efficiency and a reduced Bill of Materials (BOM) as well as low Total Cost of Ownership (TCO).

Applications driven by efficiency and TCO, such as hyper-scale data centers and telecom base stations, benefit from the switching loss reduction offered by CoolMOS C7. Efficiency gains of 0.3% to 0.7% in PFC and 0.1% in LLC topologies can be achieved, leading to significant TCO benefits. In the case of a 2.5 kW server PSU, for example, using 600 V C7 MOSFETs can result in energy cost reductions of ~10% for PSU energy loss.

In BOM and cost-driven designs such as enterprise servers, the 600 V CoolMOS™ C7 devices offer a cost reduction in magnetics. Due to the significantly lower gate charge and output capacitance, the C7 can be operated at double the normal switching frequencies with only a marginal loss in efficiency. This allows the size of magnetic components to be minimized, lowering the overall BOM cost. For example, doubling the switching frequency from 65 kHz to 130 kHz may reduce the magnetic component cost by as much as 30%.

2.2.2 CoolSiC™ Shottky diode Gen5

Selection of the boost diode is a major design decision in a CCM boost converter, because the diode is hard-commutated at a high current and the reverse recovery can cause significant power loss, as well as noise and current spikes. Reverse recovery can be a bottleneck for high switching frequency and high power density power supplies. Additionally, at low-line, the available diode conduction duty cycle is quite low, and the forward current quite high in proportion to the average current. For that reason, the first criteria for selecting a diode in a CCM boost circuit are fast recovery with low reverse recovery charge, followed by V_f operating capability at high forward current.

Since CoolSiC™ schottky diodes have a capacitive charge, Q_c, rather than a reverse recovery charge, Q_{rr}, their switching loss and recovery times are much lower than a silicon ultra-fast diode, leading to enhanced performance. Moreover, SiC diodes allow higher switching frequency designs. Hence, higher power density converters are achieved. The capacitive charge for SiC diodes is not only low, but also independent of di/dt, current level and temperature, which is different from silicon diodes that have strong dependency on these conditions.

The recommended diode for CCM boost applications is the 650 V CoolSiC™ schottky diode Gen5, which includes Infineon's Leading Edge (LE) technologies, such as a diffusion soldering process and wafer-thinning

technology. The result is a new family of products that show improved efficiency over all load conditions, resulting from the improved thermal characteristics.

The proper current rating of the PFC diode must be calculated by considering 1.3 to 1.5 times the RMS current of the diode, which is expressed as:

$$I_{D_RMS} = \frac{P_{OUT_MAX}}{V_{IN_RMS} \cdot \eta} \times \sqrt{\frac{8 \cdot \sqrt{2} \cdot V_{IN_RMS}}{3 \cdot \pi \cdot V_{OUT}}} = \frac{800}{90 \cdot 0{,}885} \times \sqrt{\frac{8 \cdot \sqrt{2} \cdot 90}{3 \cdot \pi \cdot 405}} = 4{,}1\ A$$

In this demo board, a 6 A IDH06G65C5 diode is used.

2.2.3 EiceDRIVER™ 2EDN non-isolated gate driver for MOSFETs

2.2.3.1 Introduction

The 2EDN7x24 is a non-inverting fast dual-channel driver for low-side switches. Two true rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure the highest flexibility and cover a wide variety of applications.

All inputs are compatible with LV TTL signal levels. The threshold voltages (with a typical hysteresis of 1 V) are kept constant over the supply voltage range.

Since the 2EDN7x24 is particularly aimed at fast-switching applications, signal delays and rise/fall times have been minimized. Special effort has been made to minimize delay differences between the two channels to very low values (typically 1 ns).

The 2EDN7x24 driver used in this demo board comes in a standard PG-DSO-8 package.

2.2.3.2 Driver outputs

The two rail-to-rail output stages realized with complementary MOS transistors are able to provide a typical 5 A of sourcing and sinking current. The on-resistance is very low with a typical value below 0.7 Ω for the sourcing p-MOS and 0.5 Ω for the sinking n-MOS transistor. The use of a P-channel sourcing transistor is crucial for achieving real rail-to-rail behavior and not suffering from the source follower's voltage drop.

Gate drive outputs are held low for floating inputs (ENx, Inx) or during start-up or power-down, once Under Voltage Lockout (UVLO) threshold is not exceeded.

2.2.3.3 Under Voltage Lockout (UVLO)

The UVLO function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. Therefore it can be guaranteed that the switch transistor is not operated if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation.

The default UVLO level is set to a typical value of 4.2 V or 8 V (with some hysteresis). For higher levels, such as HV SJ MOSFETs, a minimum active voltage of 8 V is used (2EDN7424), while the 4.2 V is used for the logic level driven LV MOSFETs (2EDN7524).

2.2.4 EiceDRIVER™ 1EDI galvanically isolated single-channel driver

The 1EDI driver family is based on Infineon's coreless transformer technology, enabling a benchmark minimum setting Common Mode Transient Immunity (CMTI) of 100 kV/µs.

The 1EDI20N12AF driver provides output currents of up to 2 A on separate output pins for applications up to 1200 V. They are ideal for the use in charge stations for electric vehicles as well as power supplies for servers, and industrial and telecommunications systems.

Due to lower inductive losses, these drivers enable an additional gain in efficiency of 0.5% with the latest generation of CoolMOS™ C7.

2.2.5 OptiMOS™ 5 40 V

OptiMOS™ 5 40 V, Infineon's latest generation of power MOSFETs, is optimized for SR in SMPSs such as those found in servers and desktops. The OptiMOS™ 5 40 V product family not only features the industry's lowest $R_{DS(ON)}$ but also a perfect switching behavior for fast-switching applications. 15% lower $R_{DS(ON)}$ and 31% lower Figure of Merit (FOM) ($R_{DS(ON)} \times Q_g$) compared to alternative devices has been realized by advanced thin wafer technology.

2.2.6 XMC™ for digital control

2.2.6.1 XMC1400 for PFC control implementation

The XMC1400 is part of the XMC™ microcontroller family from Infineon Technologies. This family of microcontrollers, based on ARM™ Cortex™–M0 cores, is designed for time-critical applications. The control of power supplies is a strong focus for XMC™ microcontrollers, where users can benefit from features such as analog comparators, PWM timers, co-processors or high-precision analog-to-digital converters.

Some of the XMC1400 features are listed here:

- 12-bit ADC, 1 MSample/s; flexible sequencing of conversions including synchronization
- Clock frequency is 48 MHz; nevertheless, key peripherals can run at double the CPU frequency, like PWM timers or MATH co-processors, to accelerate calculations or improve PWM resolution
- Fast analog comparators for protections such as OCP
- Co-processor that can run in parallel to the main core (Cortex™-M0); in this particular case it will help execute faster divisions (17 clock cycles)
- Flexible timing scheme due to CCU timers; these timers allow synchronization of PWM patterns and accurate generation of ADC triggers
- Interconnection matrix to route different internal signals from one peripheral to another: as an example, the timers can connect to an ADC to signify the exact point in time when a signal must be sampled, or a comparator output can be connected to a PWM timer; this can be used to make sure that whenever the comparator trips, the PWM stops

Serial communication protocols are supported, including UART, I_2C and SPI. These can be used for GUI or possible communication with the secondary stage of a full power supply.

2.2.6.2 XMC4200 for LLC control implementation

All XMC4000 devices are powered by ARM® Cortex®-M4 with a built-in DSP instruction set. The single precision floating point unit, Direct Memory Access (DMA) feature and Memory Protection Unit (MPU) are state-of-the-art for all devices – even the smallest XMC4000 runs with up to 80 MHz in core and peripherals. It comes with a comprehensive set of common, fast and precise analog/mixed-signal, timer/PWM and communication peripherals.

Some of the XMC4200 features are listed here:

- Up to 256 kB embedded Flash with 22 ns access time and error correction unit

- Up to 40 kB embedded RAM
- 8-channel DMA
- 4-channel high-resolution PWM (150 ps)
- Two ADCs with up to 8 channels each; each channel has 12-bit resolution, selectable reference and total conversion time of less than 500 ns
- Two DACs of 12-bit resolution
- Four multi-functional serial interface channels configurable to SPI, I_2C, I_2S or UART
- Two CAN nodes and USB 2.0 module
- Extended temperature range up to 125°C ambient temperature

2.2.7 QR controller (CoolSET™)

Integrated power management IC with 800 V avalanche rugged CoolMOS™, start-up cell and QR current mode flyback PWM controller in DSO-16/12 package. Suitable for 25.5 W SMPS design. The QR CoolSET™ series continues to deliver design agility and miniaturization. This new series offers the possibility of higher efficiency and better EMI performance. The digital frequency reduction feature ensures a very stable operation with decreasing load change, and the fold-back correction keeps the maximum power limits within the tolerance desired by SMPS designers. The Active Burst Mode (ABM) operation during low power consumption provides best-in-class power consumption during standby.

2.3 Board description

Figure 3 shows a top view of the 800 W server power supply. The distribution on the PCB of the different stages that comprise the PSU is highlighted: AC input and EMI filter, PFC stage, LLC (DC-DC) stage and DC output, bias (auxiliary) power supply and control board.

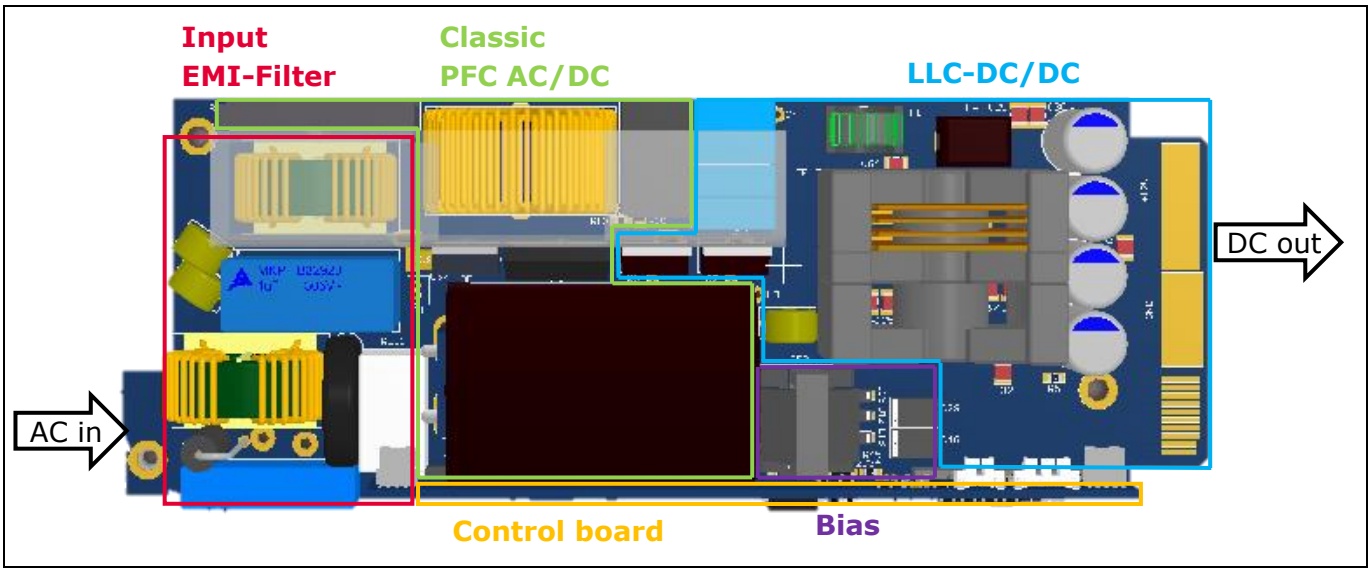

Figure 3 Distribution: top view of the different stages of the 800 W server power supply

A bottom view of the same PCB is shown in Figure 4, which shows the distribution of the drivers for both the AC-DC and DC-DC stages, as well as the SyncRec and ORing switches.

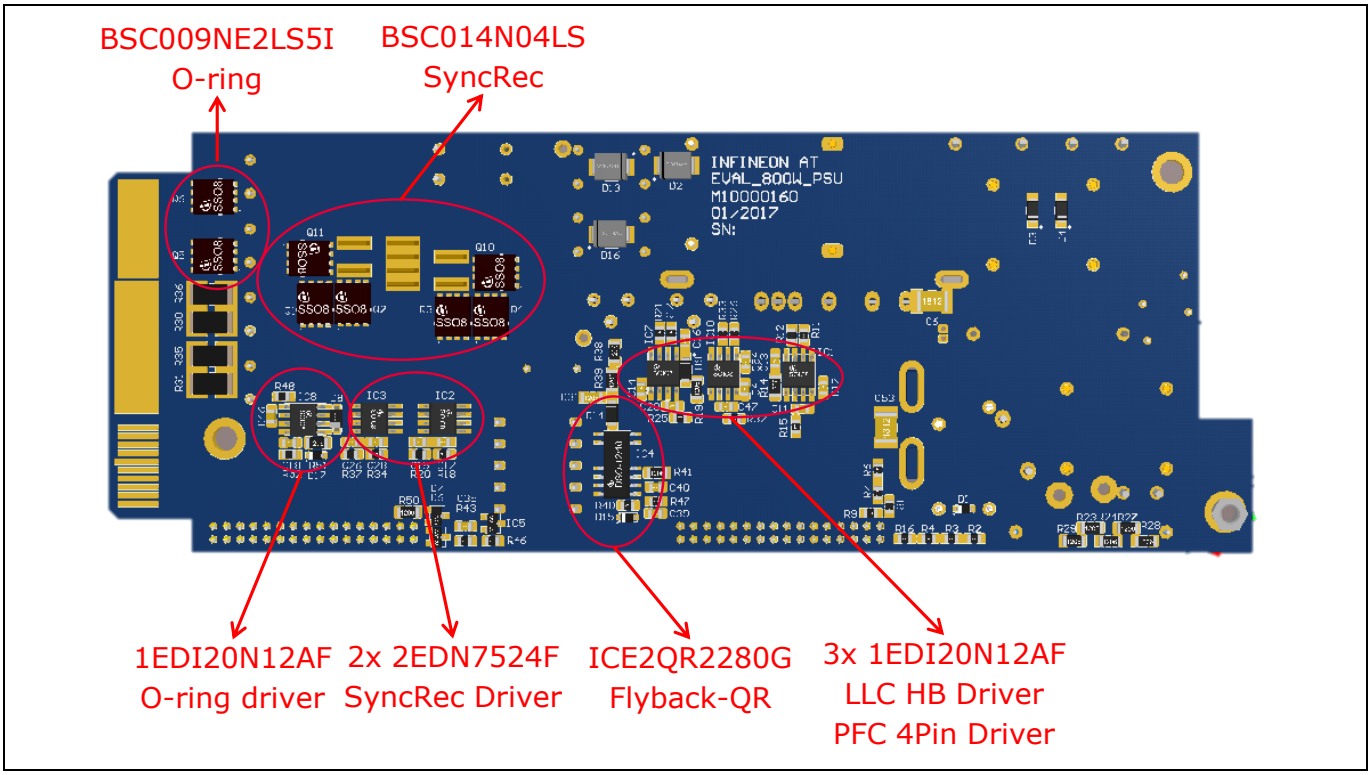

Figure 4 Bottom view of the 800 W server power supply main board

A view of the control card present on the side of the PSU is shown in Figure 5, where the XMC™ microcontrollers selected for primary- and secondary-side control are shown, together with the digital isolator. The control card is designed to support PFC monitoring and PMBus communication. However, these functionalities have not been implemented in the final current power supply.

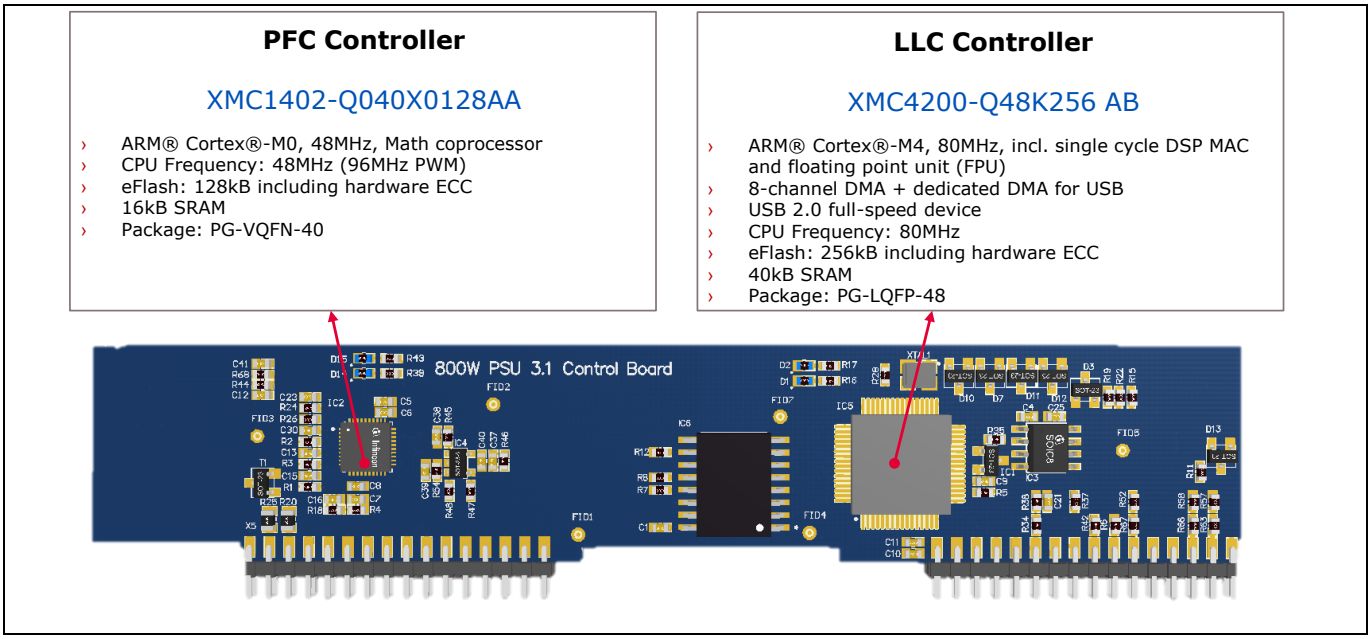

Figure 5 Control board of the 800 W server PSU with the XMC™ microcontrollers and their main characteristics

In order to demonstrate the high-efficiency performance and good regulation control under dynamic conditions (load-jumps) of the board as in a real application, an external connector PCB has been included. This gives access to the power connections and different external signals as well as containing a 2200 µF capacitor, which simulates the load behavior of the different PoL voltage regulators in a server mother board. Figure 6 shows the mentioned connector PCB with the main connections:

- 12 V and GND are the connections of the 12 V DC output
- 12 V sense and GND sense can be used for output sensing in external equipment, and this is the voltage used for 12 V DC regulation
- The included switch allows turning on and off of the PSU

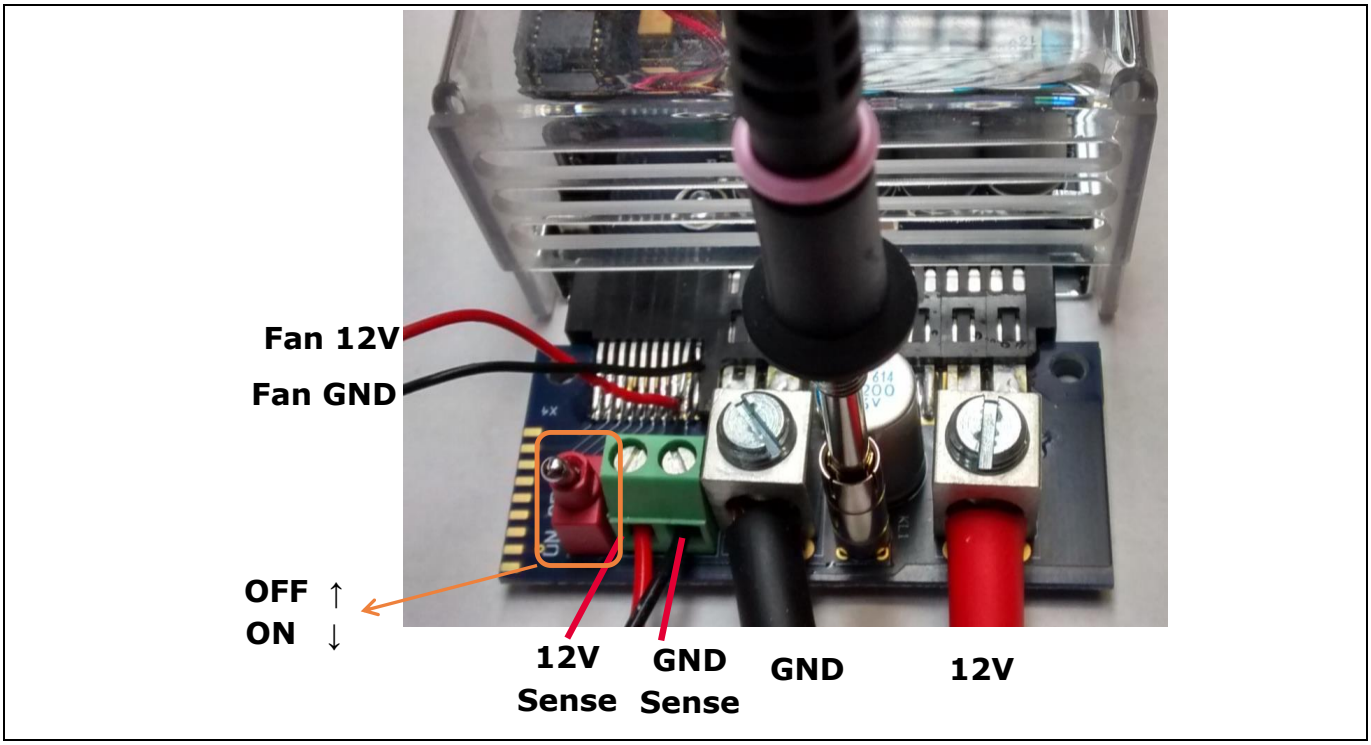

Figure 6 Output connector PCB with the main available connections

The fan included in the 800 W server PSU is supplied from the 12 V DC output of the power supply. The external connector PCB enables the connection of the output voltage terminals to the fan supply. However, external fan supply is possible by directly accessing the connector pin. In that case, the second pin of the signal connector (fan 12 V in Figure 7) must be lifted to provide the proper fan supply voltage.

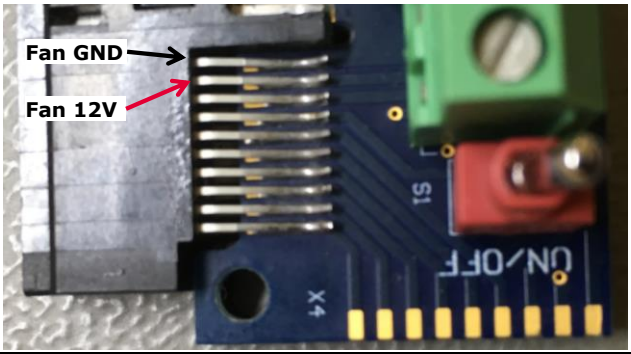

Figure 7 Fan supply connections in the output connector board

3 Power factor correction stage

The AC-DC stage of the 800 W server power supply is a classic PFC boost converter. Figure 8 shows the implemented topology, which uses a single 600 V CoolMOS™ C7 MOSFET, a 650 V CoolSiC™ schottky diode Gen5 and a 1EDI EiceDRIVER™. The Infineon microcontroller XMC1402 is used for the PFC control implementation.

The boost converter is operated at 65 kHz and provides, from universal AC input voltage range, a regulated bulk voltage to the DC-DC converter stage of around 395–405 V. The active PFC functionality is implemented in this AC-DC stage in order to demand a high-quality current waveform from the grid, according to the input requirements specified in the previous section.

This section describes the main design parameters of the implemented PFC as well as the digital control used for such functionality, with special focus on the influence of the power stage design in the control loop design and realization.

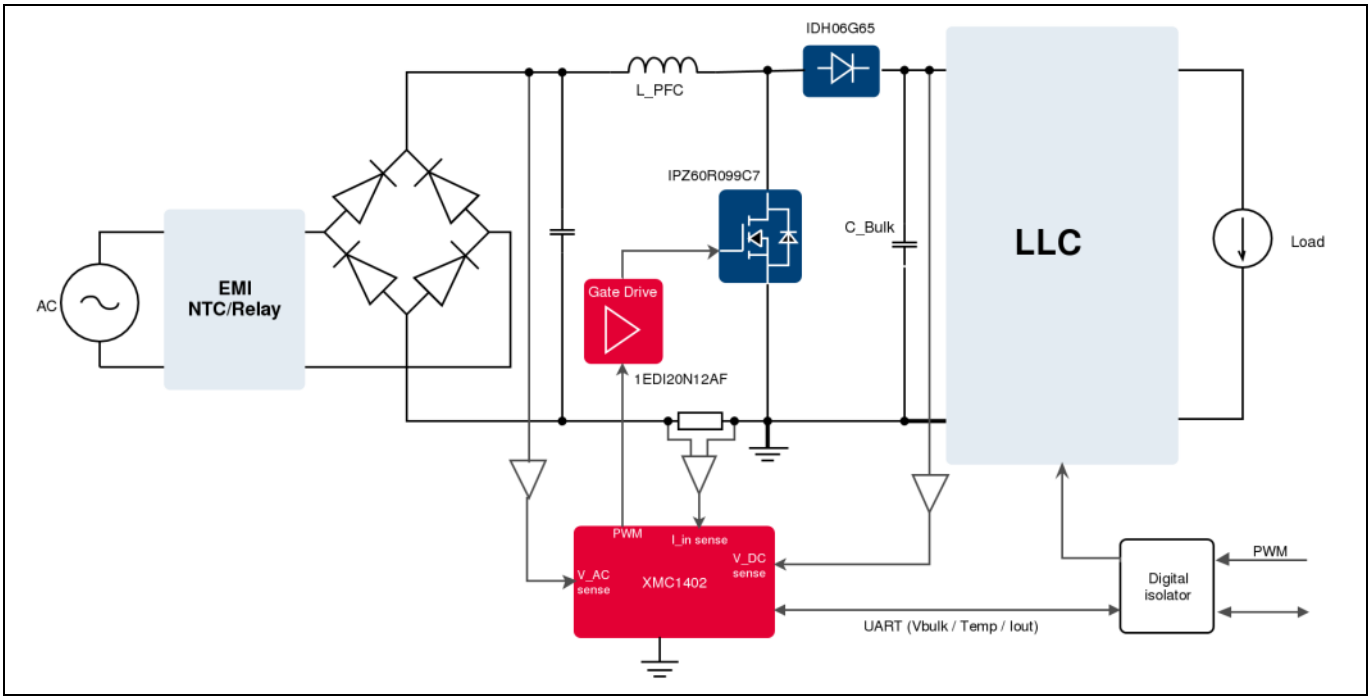

Figure 8 800 W PSU PFC topology with sensing and Infineon devices

3.1 EMI filter and rectifier bridge

The EMI filter is implemented as a two-stage filter, as shown in Figure 9, which provides sufficient attenuation for both Differential Mode (DM) and Common Mode (CM) noise.

The two high-current CM chokes L_cm are based on high permeability toroid ferrite cores. Both CM chokes implement two windings with 29 turns each, thus leading to a minimum inductance of 4 mH at each side. The relatively high number of turns, together with the winding strategy, causes a considerable amount of stray inductance. This stray inductance ensures sufficient DM attenuation.

According to the average and RMS currents through the rectifier bridge [1]. the rectifier LVB2560 with very low forward voltage drop was selected. This 800 V device also has sufficient voltage reserve, with V_{in} = 265 V.

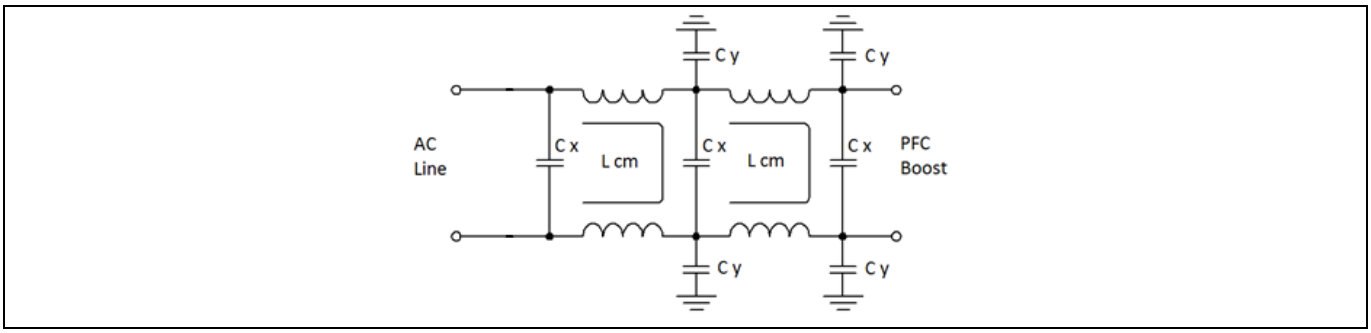

Figure 9 Two-stage filter structure

3.2 PFC choke and bulk capacitor

The PFC choke design is based on a toroidal high-performance powder core. Toroidal chokes have a large surface area and allow a good balance, minimizing core and winding losses, and achieving a homogeneous heat distribution without hot spots, hence they are suitable for systems that are targeting the highest power density with forced air-cooling.

The core material chosen was Chang Sung Corporation's HS, which has a good trade-off between DC bias, core losses and temperature stability, while its cost is lower than for HighFlux. The part number is HS270060, with an outer diameter of 27 mm and 60 µ permeability.

The built inductor has 90 turns with a small signal bias inductance of 617 µH. The effective inductance with respect to the current bias is determined by the permeability variation of the core with the DC magnetizing force (H), as illustrated in Figure 10.

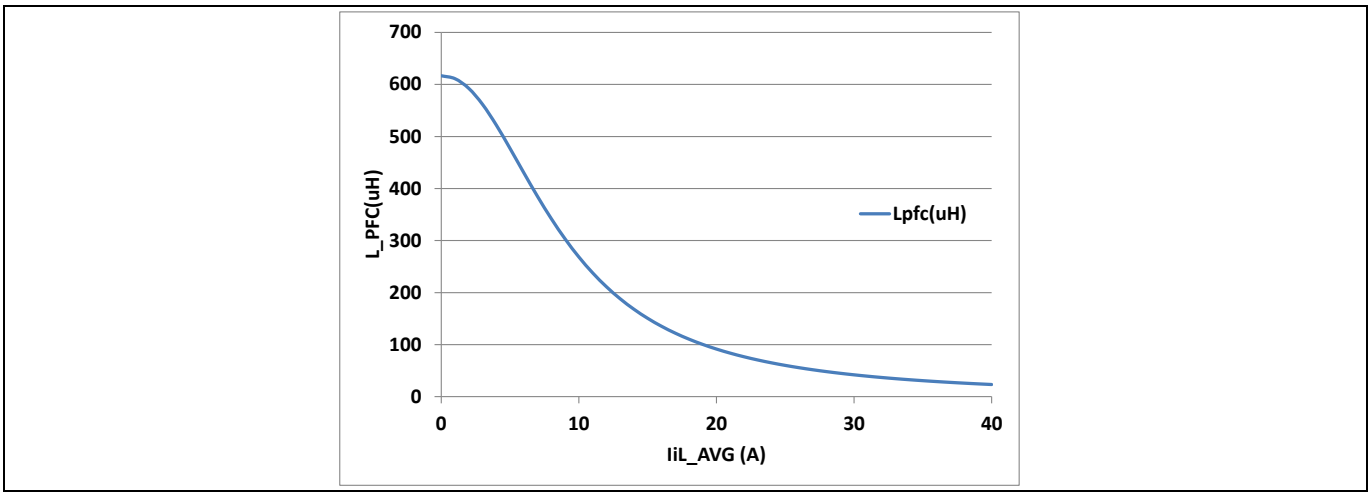

Figure 10 Inductance variation with the inductor current, linear approximation

The bulk capacitor (C_bulk in Figure 8) is typically designed according to the minimum allowable bulk voltage for a given hold-up time, i.e. the time for which the power supply must provide stable output voltage while the grid voltage is zero [1]. A 470 µF 450 V electrolityc capacitor is mounted in the 800 W server power supply, which provides a minimum voltage of 330 V for a hold-up time of 10 ms at full-load.

3.3 Functional description and control implementation

The AC-DC stage of this 800 W power supply performs PFC by a digital implemention of an average current control, in a classic Continuous Conduction Mode (CCM) boost converter. Figure 11 shows the control block

diagram, which corresponds to a typical two-loop approach, with line feedforward, used in average current control [2]. The blocks shown are implemented within software (SW).

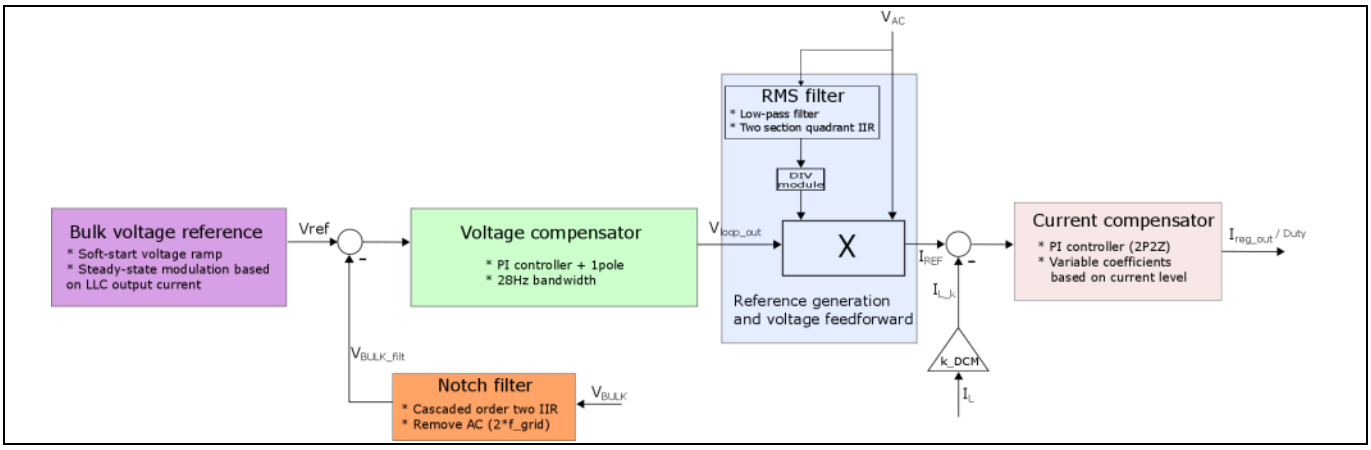

Figure 11 800 W PSU PFC control scheme

These SW blocks are shown in blue in Figure 12, together with the required HW peripherals (red) for proper operation of the PFC stage. The peripherals used can be summarized as follows:

- Three CCU8 slices: two slices configured in compare mode to generate the PWM for the PFC switch and ADC trigger; one slice used in capture mode for conduction time acquisition in Discontinuous Conduction Mode (DCM)
- Three CCU4 units used as Fixed Frequency (FF) interrupt triggers and reference generation for the analog comparators
- Two analog comparators: one for Peak Current Limitation (PCL) using the CCU8 trap functionality, and one for Zero Current Detection (ZCD) during DCM operation
- Division unit of the math coprocessor: the use of this peripheral allows a reduction in the division computation up to four times in respect to the standard SW implementation
- Four ADC channels with two different triggers for synchronized voltages and Current Sensing (CS)

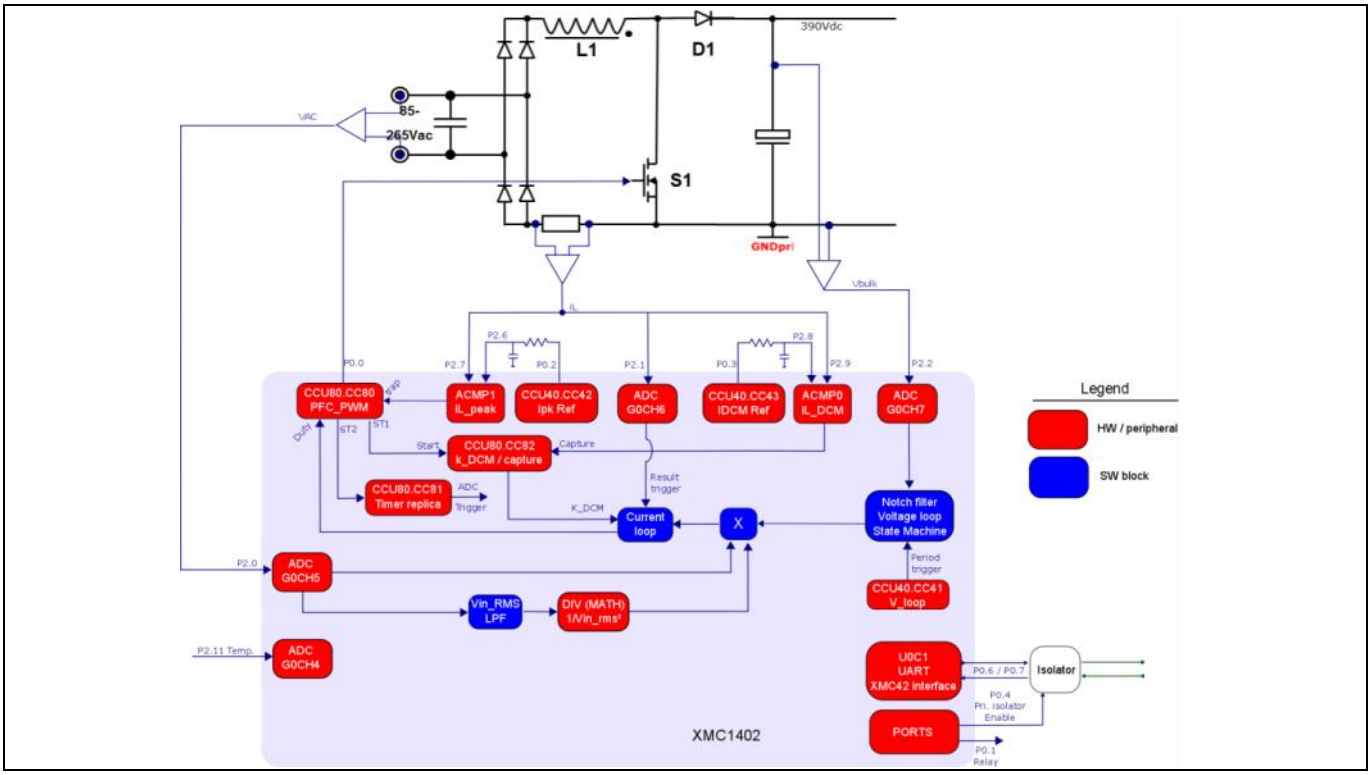

Figure 12 Peripherals and SW blocks used in the PFC of the 800 W server power supply

The CCU8 unit available in the XMC1402 microcontroller is a two-channel capture-compare unit. The possibility of using these two channels independently, together with the versatilty of the ADC and the programmable signal conditioning between the timer and ADC modules, allows a synchronized and noise-free sensing of the necessary voltages and currents for PFC operation.

Figure 13 shows the time diagram of the ADC sensing and Interrupt Service Routine (ISR) trigger of the implemented current loop, which is executed every switching cycle (f_{sw} = 65 kHz). Compare channel 1 (CR1) of the main timer (PFC PWM) carries the duty cycle information. However, compare channel 2 (CR2) is set to half of the CR1 value to trigger the ADC queue [3]. Therefore, the inductor current is sensed in half of the on-time, which corresponds to the inductor current average value in CCM operation. The result event of the ADC is used to trigger the current control ISR, which ensures using the last acquired current value.

At the same time, a second timer (timer replica) is synchronized with the main timer. The use of the replica allows synchronization as well the bulk voltage measurement. In this case, a second ADC group, e.g. the scan ADC [3], is triggered in the middle of the off-time, thus reducing the sensing noise.

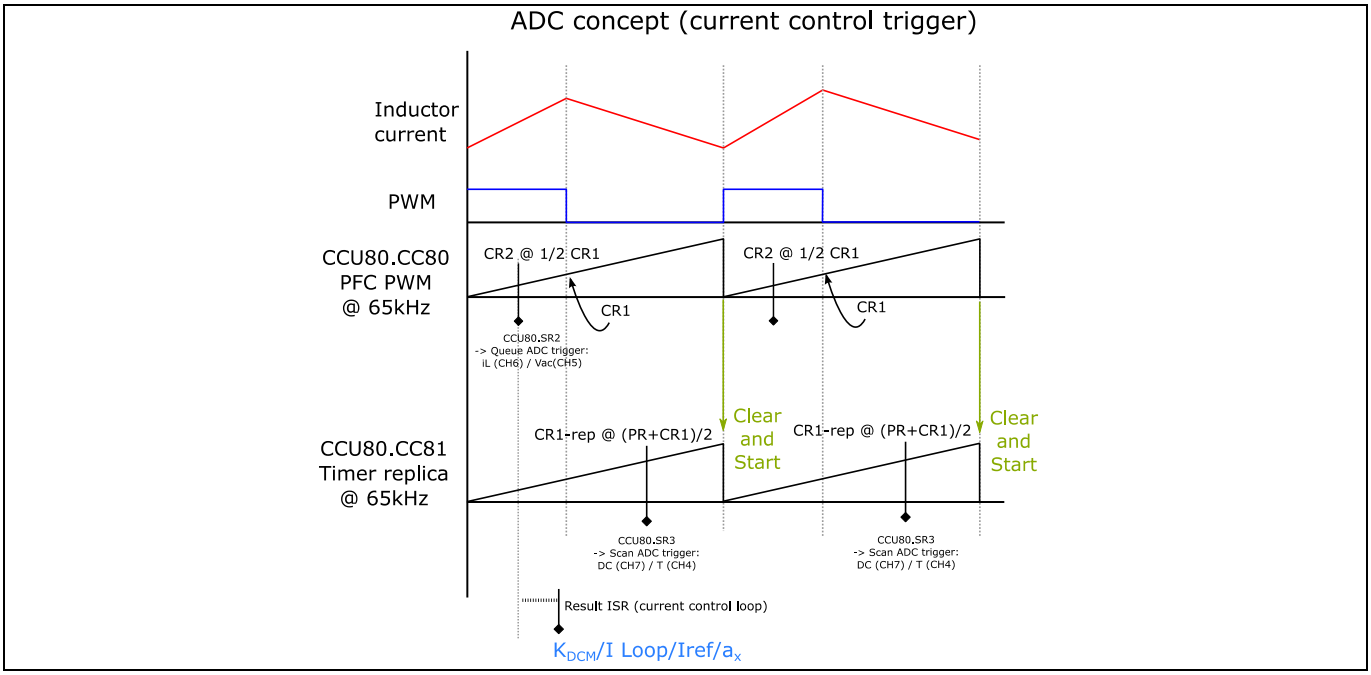

Figure 13 Timers and ADC synchronization in the implemented PFC control scheme

The voltage-loop, PFC state machine, Low Pass Filter (LPF) of the input voltage and bulk voltage notch filter are implemented in a second ISR triggered at an FF of 6.5 kHz using a CCU4 slice. The scheduling of these functionalities is shown in Figure 14.

Both the AC filter (LPF of the AC voltage) and the notch filter of the bulk voltage are two cascaded sections of second-order IIR filters.

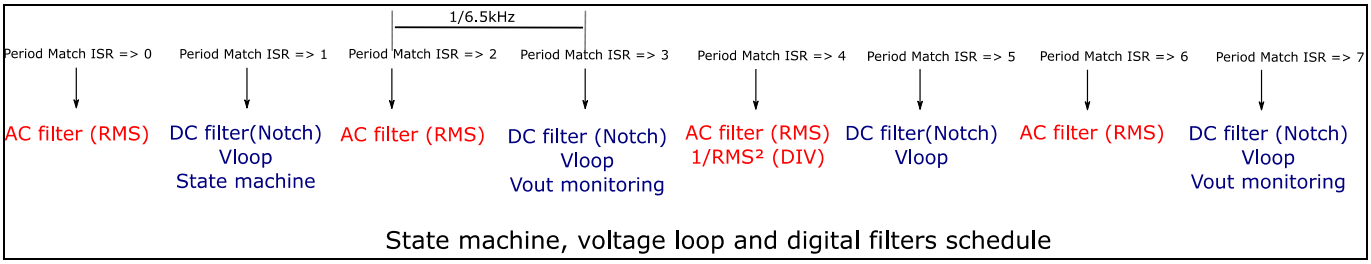

Figure 14 Time schedule of the voltage loop interrupt at 6.5 kHz

The state machine (Figure 15) ensures the correct behavior of the PFC systems by controlling the start-up phase and monitoring the output and input voltage during operation. During start-up the relay is closed before the boost converter starts switching, in order to bypass the NTC resistance which limits the inrush current. The relay is then open only in case the bulk voltage goes under a defined level, under which the PFC is restarted.

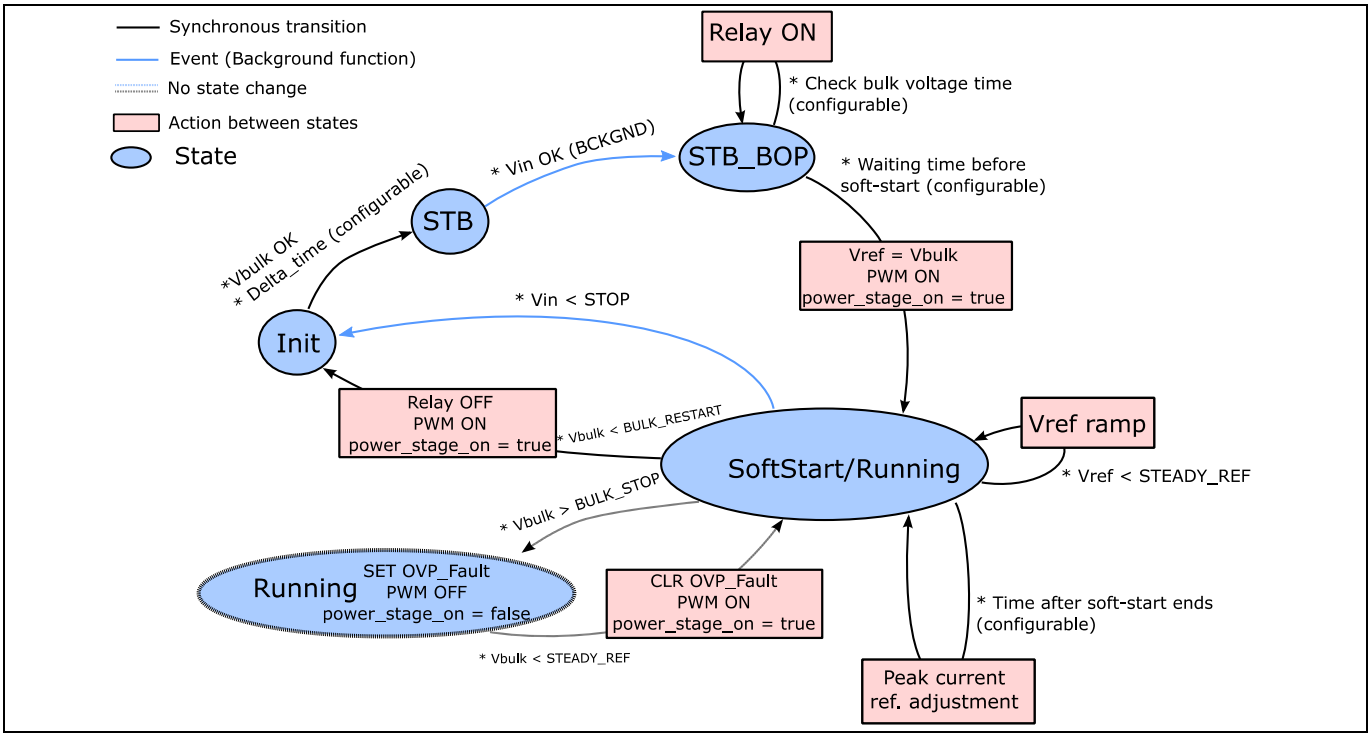

Figure 15 PFC state machine

3.3.1 Current controller

The design of the current controller in a PFC boost converter in CCM operation is well known for both analog and digital implementation, using PI or PID controllers and with or without duty cycle feedforward [1, 2]. Nevertheless, different issues such as inductance variation of the saturable inductor, DCM operation and filter interactions arise during the PFC operation.

- Saturable core inductance variation in the PFC current loop

According to the references given, the gain of the control to inductor current transfer function (G_{id}) is inversely proportional to the inductance value. In the PFC choke design shown, a saturable core is used and so the inductance changes as shown in Figure 10. This inductance variation implies a gain change according to the average current, i.e. a change in G_{id} during the AC half-cycle. Therefore, if a single controller is used for all the operating conditions, BW variations will occur with the risk of instability, as shown in Figure 16.

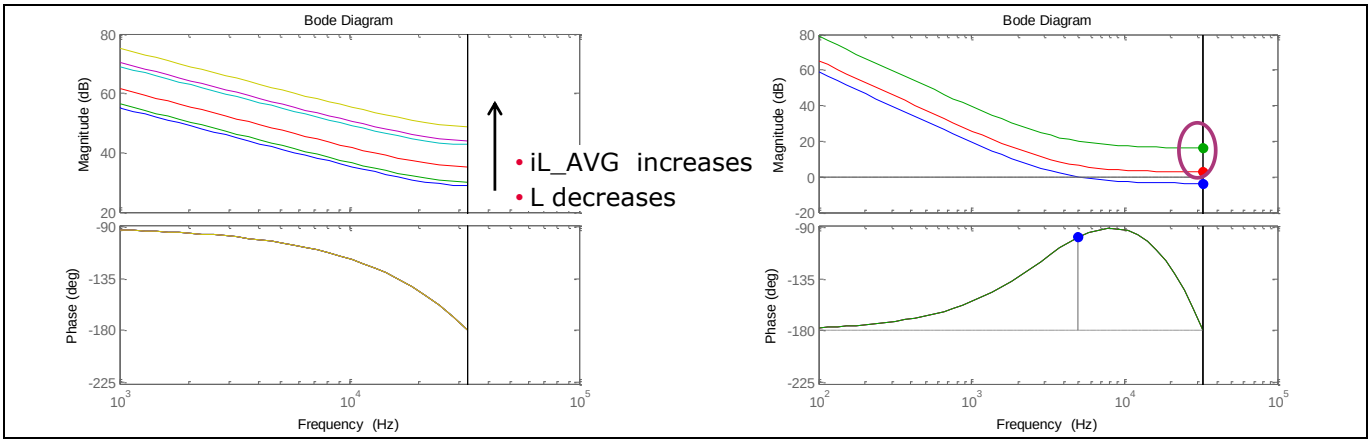

Figure 16 Control to inductor current transfer function gain variation with the inductor average current (left) and instability caused by inductance change with a single controller

In the digital implementation introduced above, the controller gain is modified according to the inductance variation to maintain adequate stability margins during the half-line cycle. A linear approximation is used for the inductance variation, which is known by design. As shown in Figure 17, two different linearizations are used depending on the sensed current level (under or over 15 A). This variation is coded in the SW and used to modify the controller coefficients in the current loop ISR, according to the sensed current. As a result the BW variation is limited, thereby avoiding instabilities and enhacing the loop performance (Figure 17).

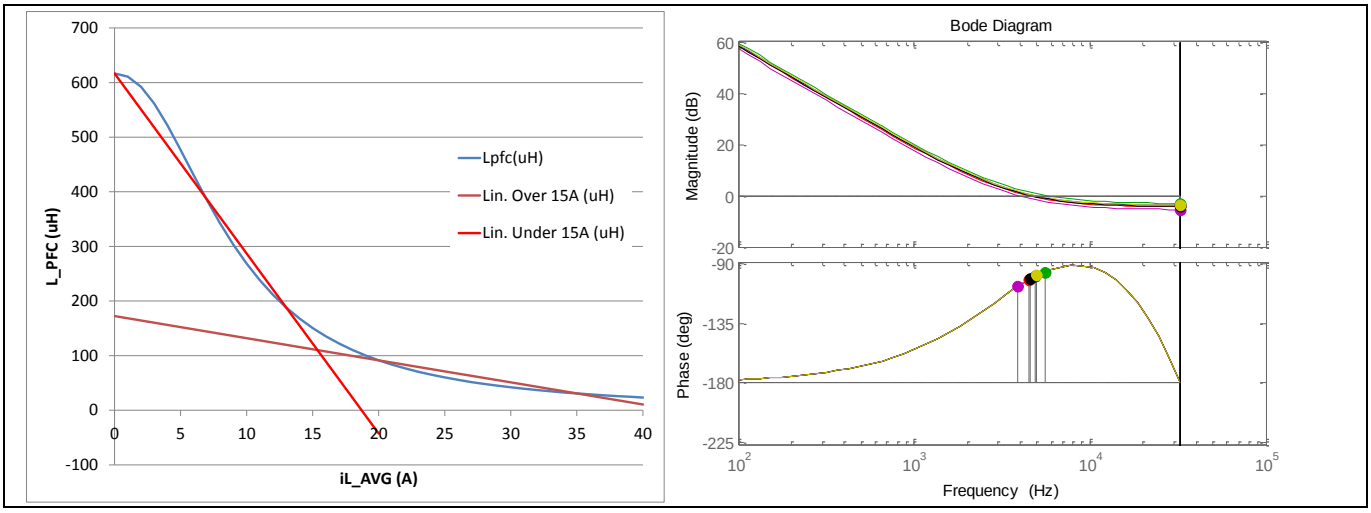

Figure 17 Inductance linear approximation (left) enables stable operation with limited BW variation during a half-line cycle (right)

- DCM operation at light load

The second issue in PFC is the change from CCM to DCM operation at light load, especially in high-line conditions. In [1] the coexistence of both operation modes during a half-line cycle is analyzed, as well as the G_{id} change between the two conduction modes. This coexistence leads to an increase of the input current distortion due to two main factors: the BW degradation of the current loop if a CCM controller is used in DCM operation, and the mis-match of the sensed current and the actual average inductor current.

The dynamics change in the boost converter operating in CCM and DCM is shown in [4]. As a consequence, if a current controller designed for CCM operation is used in DCM operation a drastic degradation of the current loop BW occurs. Figure 18 shows this performance degradation for the 800 W PSU PFC stage. In this case a current loop with a 2 kHz BW is designed for CCM operation. If the same controller is applied in DCM operation the BW is reduced to 64 Hz, leading to significant current tracking error and, therefore, an increased distortion.

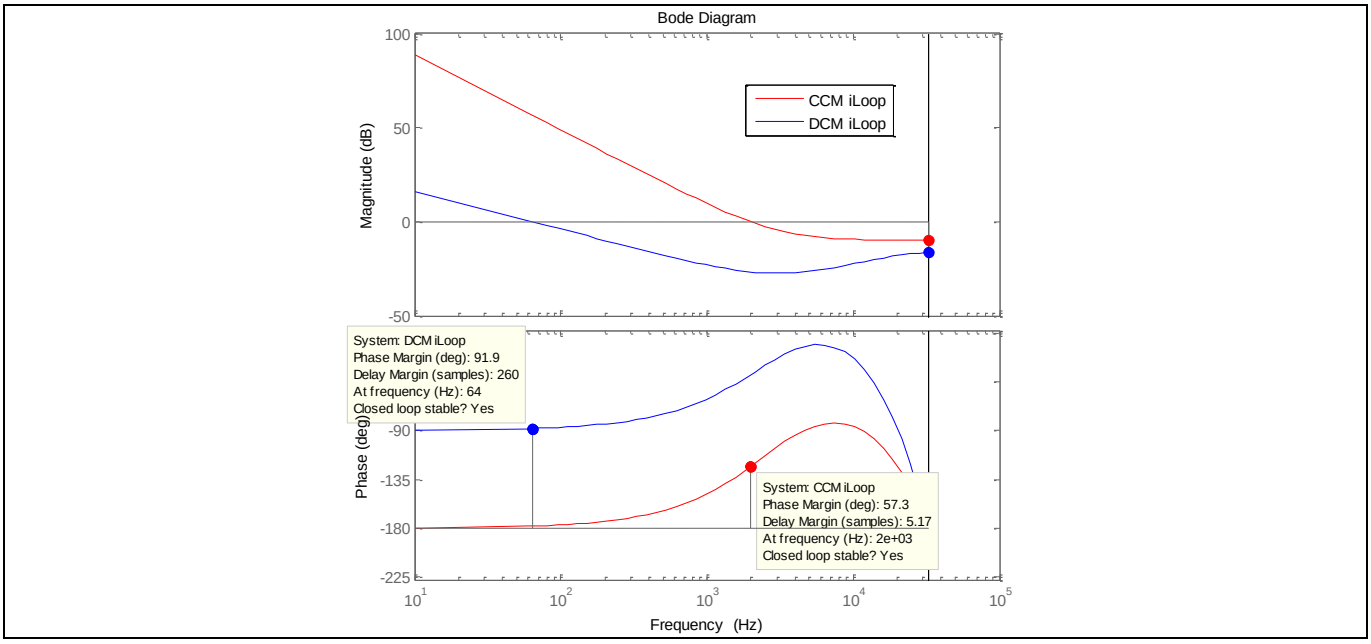

Figure 18 Inductance linear approximation (left) enables stable operation with limited BW variation during a half-line cycle (right)

In order to keep a similar BW when the converter operates in different conduction modes, the controller gain must be increased by a factor greater than 10 in DCM operation in respect to CCM. This implies a risk of instability in the change from DCM to CCM if the wrong controller is applied, which increases the complexity and accuracy in the conduction mode detection.

In the solution shown, a controller that provides a 9 kHz BW in CCM operation is applied. This BW increase enables a BW in DCM operation over 270 Hz, while no accurate DCM/CCM detection is required.

The delay in the current tracking caused by the diminished-loop BW is aggravated by the fact that the sensed current does not match the actual average inductor current. As stated above, the CS is triggered in half of the on-time, which corresponds to the average inductor current in CCM operation. However, in DCM the sensing point provides a current that is higher than the actual average current (Figure 19). This increases the already high error due to the reduced BW.

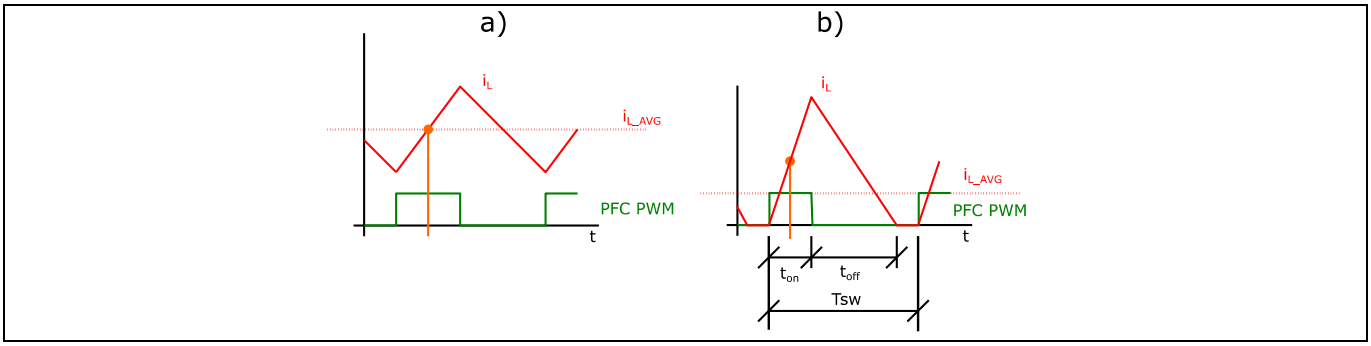

Figure 19 Average inductor current and ADC sensed value for CCM (a) and DCM (b) operation

According to the waveform shown in Figure 19 the average current (i_{L_AVG}) is proportional to the sensed current with a factor K_{DCM}, as expressed in equation (1) [4].

$$i_{L_AVG} = k_{DCM} \cdot i_{L_ADC}; \qquad k_{DCM} = \frac{t_{on} + t_{off}}{T_{sw}} \tag{1}$$

The timers present in XMC1402 can be used in compare mode, thus allowing the generation of PWM signals or ADC triggers as shown until now. In addition, the same timers can be configured in capture mode. In this case, the timer can be configured to capture the timer value when a certain event occurs.

This functionality is used to acquire the inductor conduction time (t_{on} + t_{off} in Figure 19), thus enabling calculation of the correction factor for the inductor current in DCM operation. The timer is initialized with the rising edge of the main timer. On the other side, the timer acquisition is done with the falling edge of the comparison output of the inductor current, with a fixed reference value close to zero. DACs are not available in the XMC1000 series, and a PWM with an external RC filter is used instead to generate such a reference. The required HW configuration is shown in Figure 20.

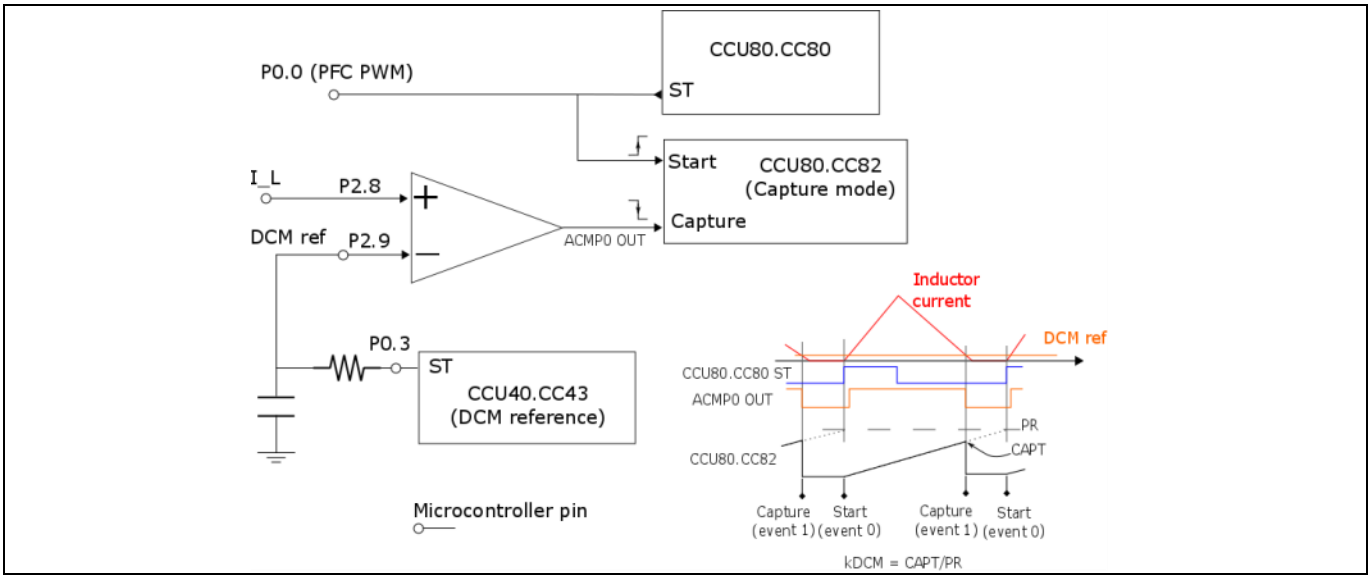

Figure 20 Inductor current conduction time acquisition using the XMC™ timer capture functionality

- Filter interactions

A third issue to consider when designing the PFC current loop are the possible interactions between the EMI filter and the boost converter. These interactions happen between the output impedance of the filter and the converter input impedance, as shown in [5].

In low-line operation the demanded current by the PFC increases, and therefore the input impedance of the boost converter decreases. Figure 21 shows the output impedance of the EMI filter together with the input impedance of the PFC converter at low-line and full-load. According to the frequency response shown, if a 9 kHz BW is applied in these operating conditions, the intersection of the impedances provokes oscillations in the input current.

Reducing the current loop BW avoids the impedance intersection, as the green curve in Figure 21 shows. Therefore, in high-current operating conditions, the controller BW is reduced to 5 kHz in order to minimize the filter interactions.

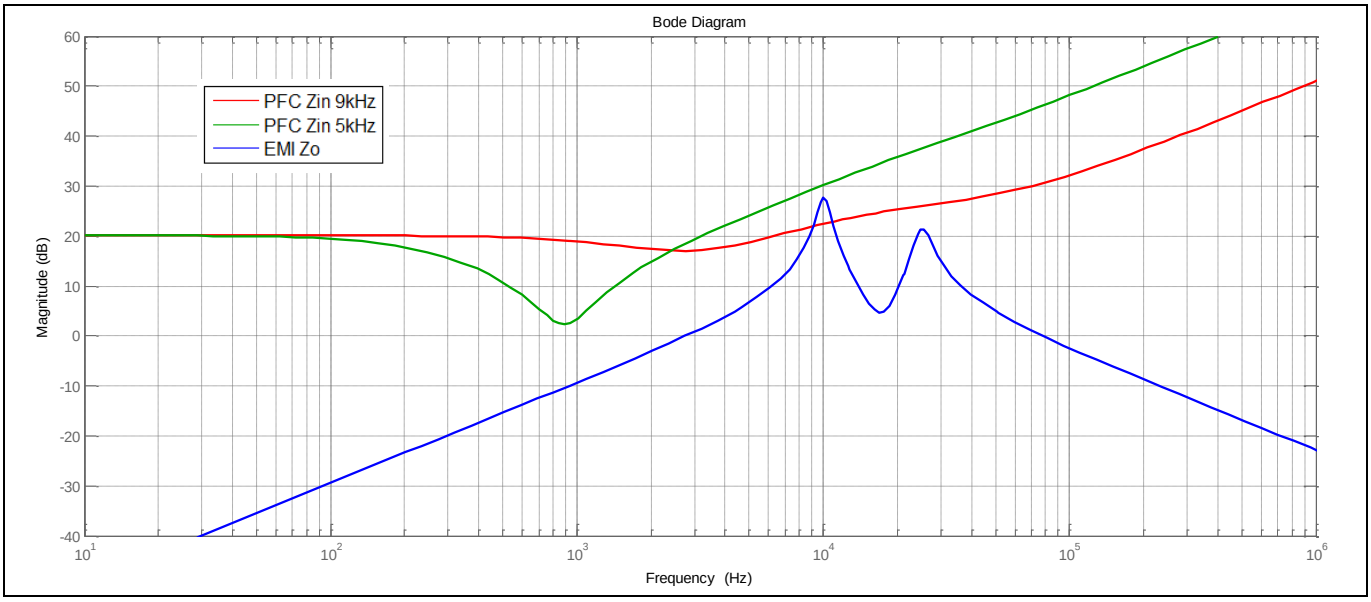

Figure 21 PFC input impedance with 9 kHz (red) and 5 kHz (green) current loop BWs as well as EMI filter output impedance (blue) for full-power operation at 90 Vrms

Figure 22 shows the BW change implementation according to the sensed average current. A high BW is kept under 6 A operation when there is no risk of filter interactions, in order to keep a good performance in terms of PF and THD. However, when the current increases the BW is reduced to minimize the current oscillations due to filter interactions. A hysteresis is applied to avoid stability problems due to continuous BW modification.

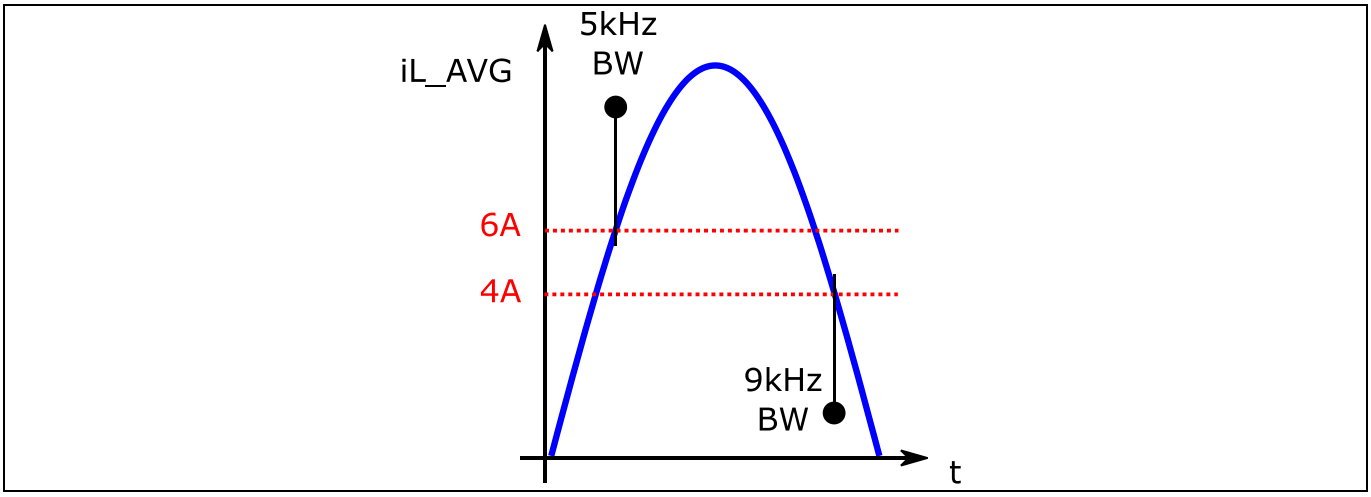

Figure 22 BW change according to current level

3.3.2 Voltage loop

In the selected control scheme, the required current reference is generated by the multiplication of the sensed input voltage, the RMS information of this same voltage, and the information provided by the voltage loop. Therefore, the voltage loop design has a direct impact not only on the adequate voltage regulation but also on the current distortion.

In order to obtain a non-distorted input current reference, the voltage loop must filter the twice-line frequency ripple present in the bulk voltage. A simple way is to use the controller itself as a filter, by reducing the loop BW (under 10 Hz). However, this option significantly jeopardizes the voltage loop regulation.

Instead, the approach used in this PFC (Figure 11) is the introduction of a highly selective filter that eliminates the twice-line frequency ripple from the sensed bulk voltage. The filtered information is then fed in the voltage loop, which enables increasing the loop BW close to 30 Hz (Figure 23).

In the selected implementation two-notch digital IIR filters tuned to 100 Hz and 120 Hz are placed in cascade formation. As a result, these two frequencies are removed from the sensed bulk voltage, as shown in the loop gain shown in Figure 23. This implementation, although computationally costly, does not require frequency detection and is robust against grid frequency changes during the converter operation.

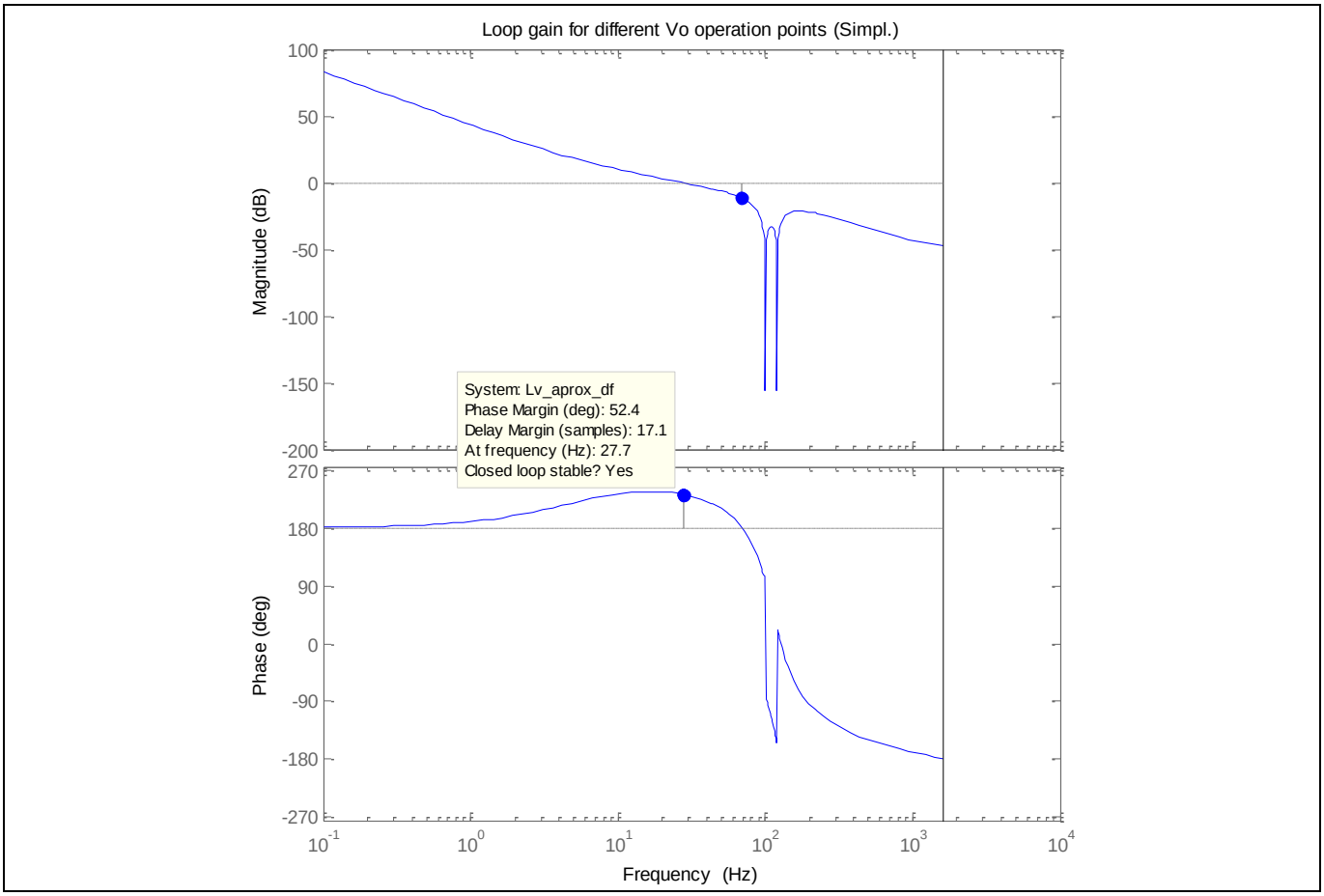

Figure 23 Loop gain of the voltage control loop

Despite the achieved BW in the proposed implementation, under certain situations such as load-jumps or PLDs the bulk voltage can over- or under-shoot, leading to different issues such as instability or maximum voltage violation. Furthermore, the bulk voltage level directly affects the DC-DC converter operation. For these reasons the bulk voltage is monitored as part of the state machine shown in Figure 15. Three main actions are implemented in this monitoring:

- In case of over-shoot (programmable level), the PWM is off until the sensed voltage returns to the target value
- If the sensed voltage is under a defined level, the current reference is increased by a factor of 4 until the sensed voltage reaches a higher limit
- In case the sensed voltage is under 333 V, the PFC is turned off and its operation is resumed with soft-start after a defined time; this causes the DC-DC converter to be turned off as well

The digital implementation also enables a modification of the PFC output voltage target according to the delivered output current/power. This voltage directly influences the DC-DC converter switching frequency, since it is a frequency-controlled resonant converter – and therefore its efficiency.

Figure 24 shows the implemented voltage target variation used in the 800 W server power supply. The output current information is sent from the secondary to the primary controller via UART through a digital isolator. As a side-effect of this implementation, a higher voltage at full power gives extra voltage in case of ACLDO.

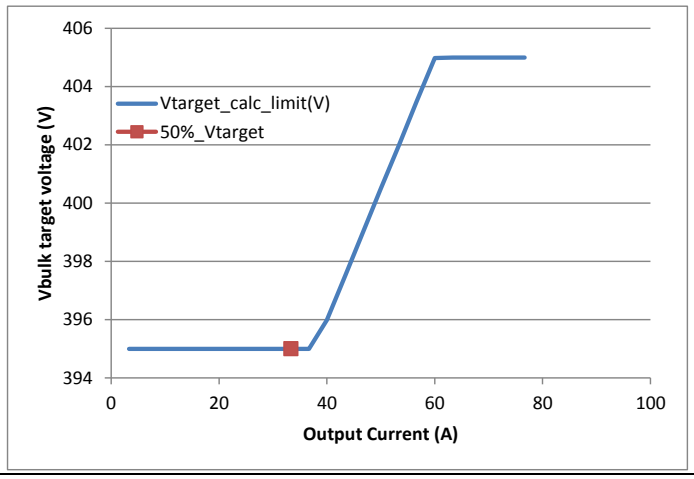

Figure 24 Bulk voltage variation for efficiency optimization

4 LLC resonant DC-DC converter

The DC-DC stage of the 800 W server power supply is a half-bridge LLC resonant converter with split capacitors and center-tap transformer configuration. The implemented topology is shown in Figure 25, which includes the 600 V CoolMOS™ C7, 40 V OptiMOS™, 1EDI and 2EDN EiceDRIVER™ and XMC4200 as controller. Since the selected microcontroller is located in the secondary side, a digital isolator is used for communication with the PFC controller. In addition, the inclusion of this digital isolator allows for sending the PWM signals to the half-bridge drivers without using pulse transformers. The DC-DC stage also includes the ORing swich.

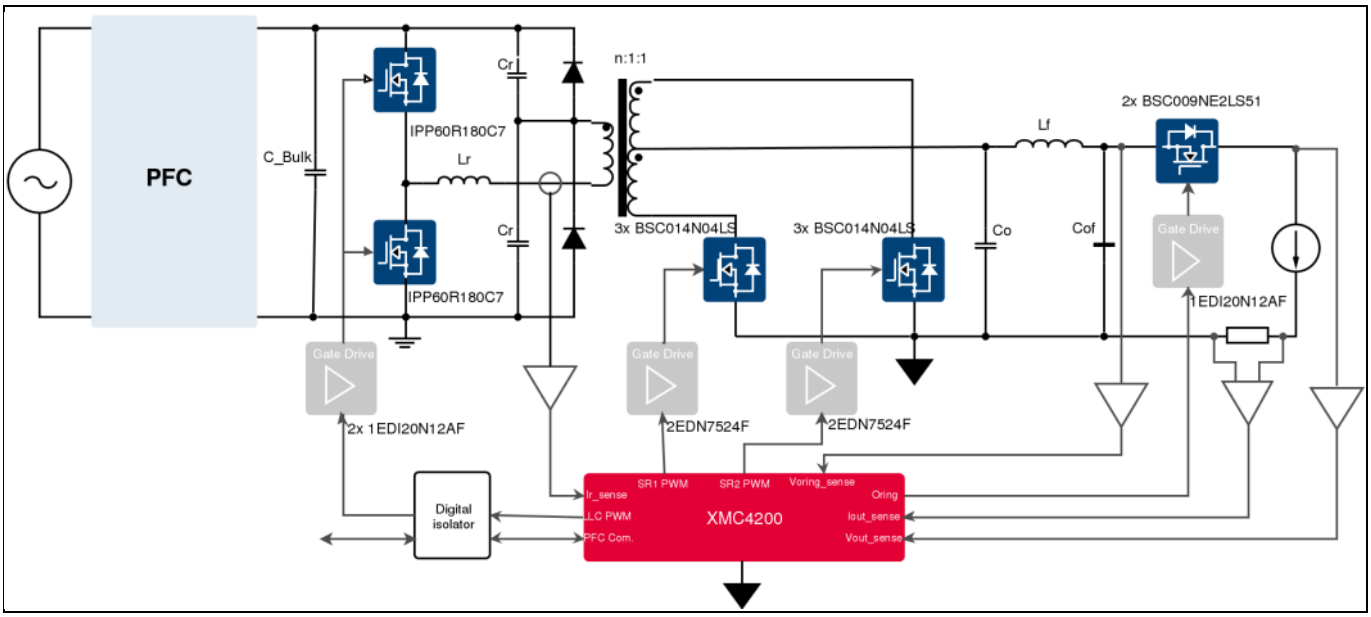

Figure 25 800 W PSU LLC topology with sensing and Infineon devices

4.1 Resonant tank design

The design of the LLC converter involves several steps in a well-defined design flow, as introduced in [6]. In the case of the server power supply described in this document, the input voltage variation is influenced by the selected bulk capacitor in case of loss of the AC input voltage. In these conditions the maximum gain of the LLC operation is required, since the lowest input voltage must be boosted to the specified regulated output voltage. With this consideration and a resonant frequency target close to 150 kHz, the resultant tank parameters are:

- Resonant inductance: Lr = 9 uH, with 1 uH coming from the stray transformer inductance
- Resonant capacitance: Cr = 132 nF, in split capacitor configuration
- Magnetizing inductance: Lm = 169 µH

Considering the parameters described, the gain curve at full-load is shown in Figure 26, together with the maximum required gain.

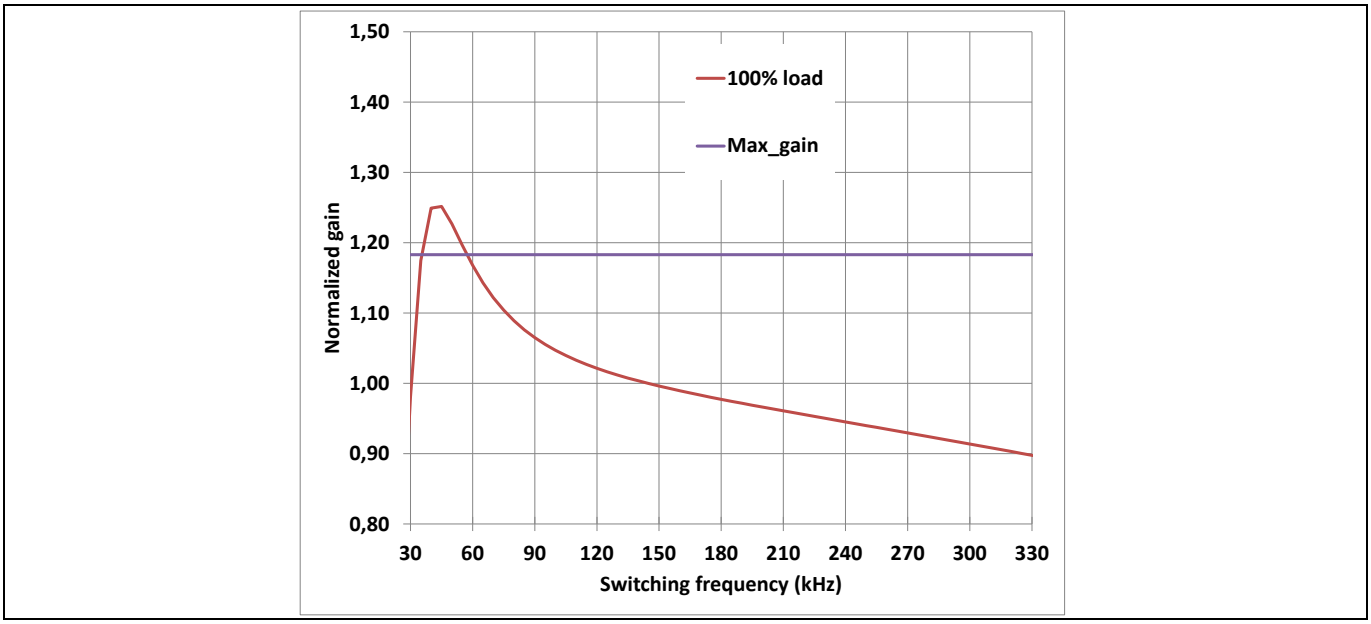

Figure 26 **Normalized gain curve at full-load and maximum required gain for the LLC converter of the 800 W server power supply**

4.1.1 Transformer and resonant inductor

The two main value drivers for the server power supply shown are high performance and power density. With these parameters in mind, the main transformer and the required resonant inductance have been integrated. The resulting magnetics integration, which takes advantage of the flux cancellation, is shown in Figure 27.

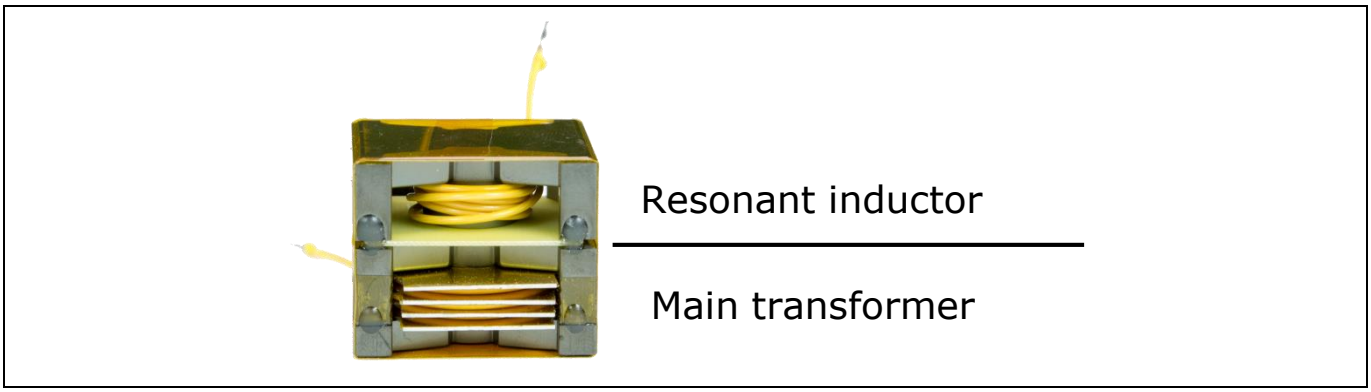

Figure 27 **Main transformer and resonant inductor integration**

The transformer and resonant inductor are both built using PQI35/23 cores. The secondary windings are implemented using 0.6 mm thickness copper foils. The primary-side turns are wound between the copper foils, thus improving the transformer coupling, using 7 × 0.3 mm litz wire. The same wire is used for the resonant inductor turns, which are in series with the primary transformer windings.

4.2 XMC™ configuration and functional description

As described in section 2.2.6.2 , the control of the DC-DC stage in the 800 W server power supply is implemented in an XMC4200. Figure 28 shows a block diagram of the HW (red) and SW (blue) resources used for the control implementation.

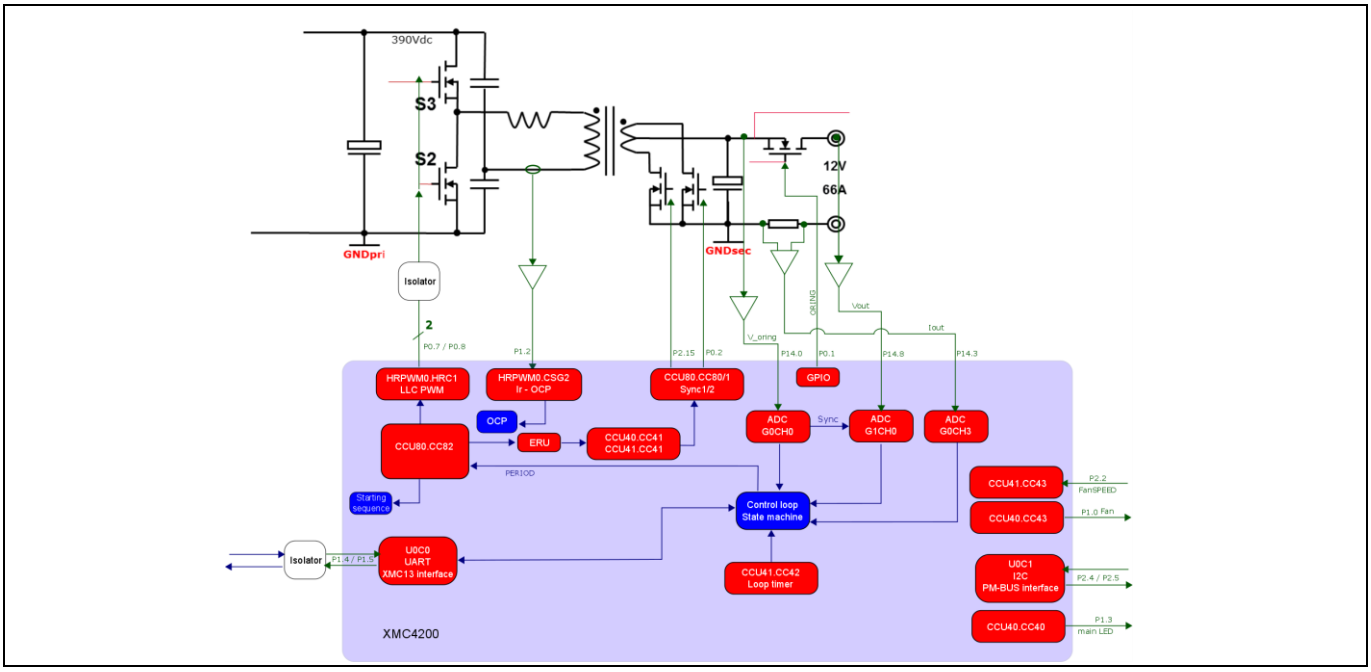

Figure 28 XMC4200 configuration for the LLC converter of the 800 W server power supply: red – HW blocks (peripherals); blue – SW blocks

As a resonant converter, the LLC requires frequency modification (60–300 kHz) in order to maintain voltage regulation. Therefore if the control loop is synchronized with the switching frequency, the necessary operations for control-loop calculation must be executed in a maximum time that corresponds to the minimum switching period. In addition, more functions than the control loop are typically implemented in the controller, which complicates the synchronization of the control and the switching frequency. This is the reason to include an FF interrupt (100 kHz) to implement the following functions, which will be covered in this section:

- Over Voltage Protection (OVP)
- OCP
- Receive information from the primary-side controller
- State machine
- Voltage controller
- Burst mode detection
- Send information to the primary-side controller

4.2.1 Sensing

Proper operation of the LLC converter requires the sensing of the output voltage, both before and after the ORing switch, since it is the variable to be controlled. In addition, the output and resonant current are necessary for OCP, and the input voltage is used for brownout protection.

- Resonant current and short-circuit protection

The resonant current is sensed using a current transformer and the signal is rectified afterwards. The obtained voltage is connected to the internal analog comparator of the high-resolution PWM module [7], which includes an internal DAC. The DAC is programmed to a constant value, which is reached only in case of short-circuit. If this comparison happens, the converter operation is frozen and a microcontroller reset will be necessary to resume operation.

- Input voltage

The microcontroller is located in the secondary-side ground, which is a problem when sensing the bulk voltage (LLC input voltage). Nevertheless, this information is available in the primary-side controller for the PFC control. The XMC4200 receives the input voltage information via UART through the digital isolator. The communication rate is fast enough for the proper operation of the brownout protection of the LLC, but slow enough to minimize noise problems in the communication.

- Output current and voltages

The rest of the mentioned variables, output voltages and current, are sensed using the ADC of the secondary-side controller. The XMC400 series ADC enables use of an external reference via channel 0 of the ADC [7]. In this case a high-accuracy 2.5 V reference is used, in order to minimize production tolerances.

Furthermore, the output voltages before and after the ORing switch are acquired at the same time by using the channel synchronization of the versatile ADC of the XMC™ microcontroller [7]. After these voltages are sensed, the output current is also acquired. The output current information is sent to the primary-side controller via UART (full-duplex) communication. This information is used to modulate the bulk voltage, as explained in the PFC section.

As in the case of the PFC, the ADC trigger is done with the second available compare register of the CCU8 unit, which is generating the half-bridge driving signal (Figure 29). With this configuration, the different variables are sensed every switching cycle in a noise-free environment.

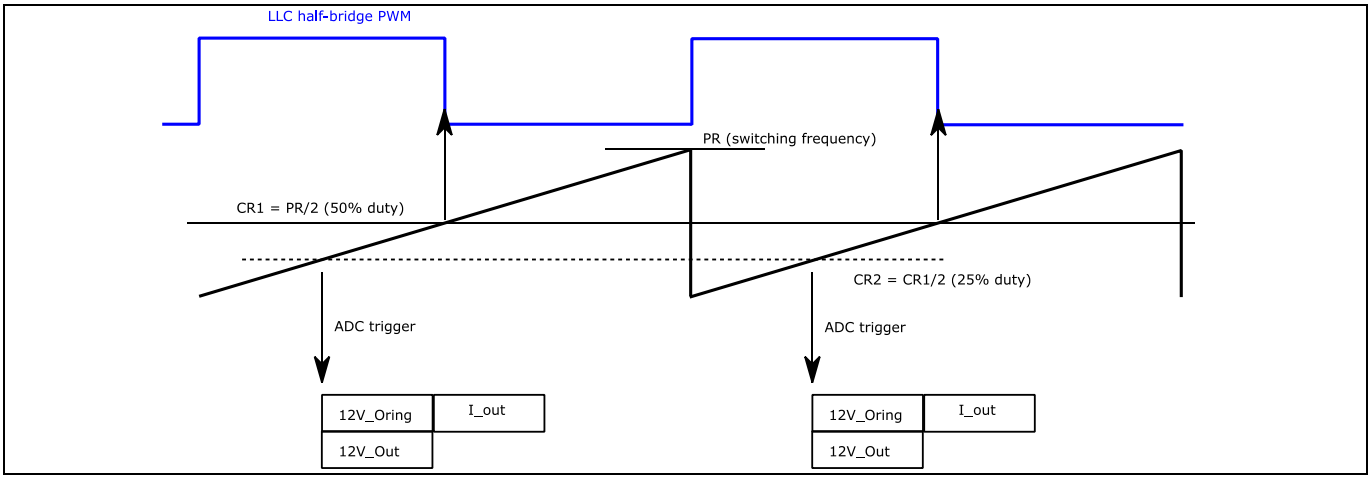

Figure 29 ADC time schedule

4.2.2 XMC™ configuration for CoolMOS™ and OptiMOS™ safe operation

The required timing for the SR switches with regard to the half-bridge operation is different if the LLC converter operates in under- or above-resonance conditions [6]. Despite the SW considering this timing, abrupt switching frequency changes might happen in case of dynamic situations, i.e. load-jumps, which in turn might lead to timing mis-match and device stress.

Different HW configurations have been implemented, taking advantage of the XMC4200 peripherals' flexibility and connectivity, in order to avoid SR cross-conduction or timing mis-match between primary and secondary driving signals in these conditions. The connection of the required timers is shown in Figure 31.

The main timer sets the switching frequency according to the voltage controller. This information is used in the high-resolution PWM module (HRPWM, Figure 31), which enables the modification of the dead-time safely and

synchronously with the frequency change. The dead-time of the half-bridge LLC is modified, as shown in Figure 30, according to the switching frequency to guarantee ZVS operation under any condition.

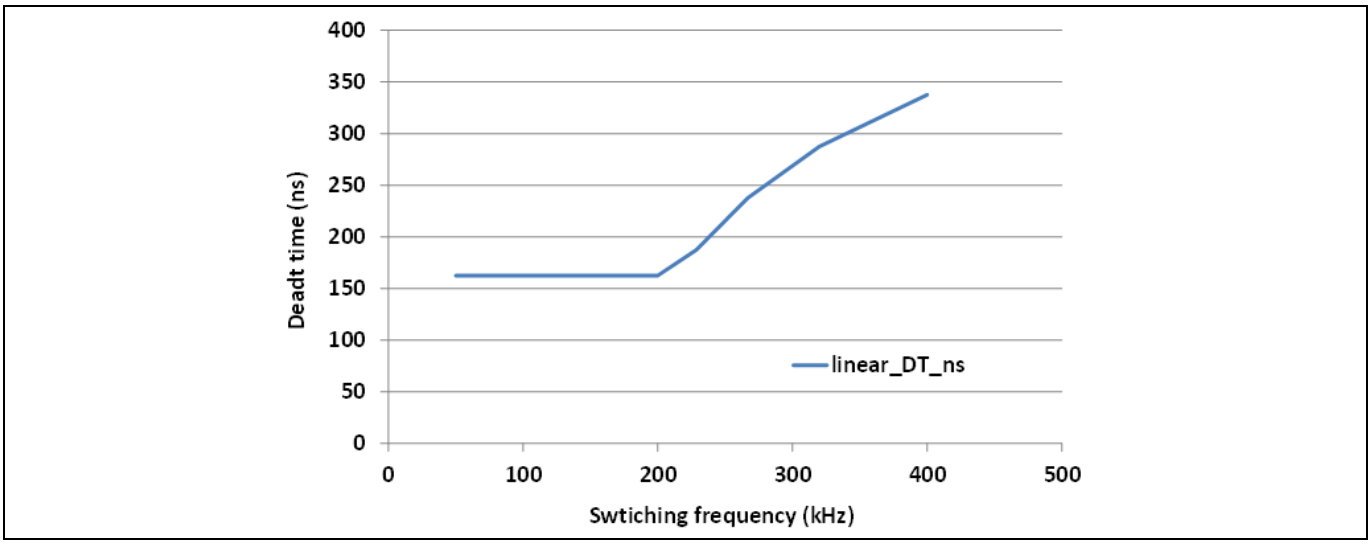

Figure 30 Dead-time modification according to switching frequency of the half-bridge LLC

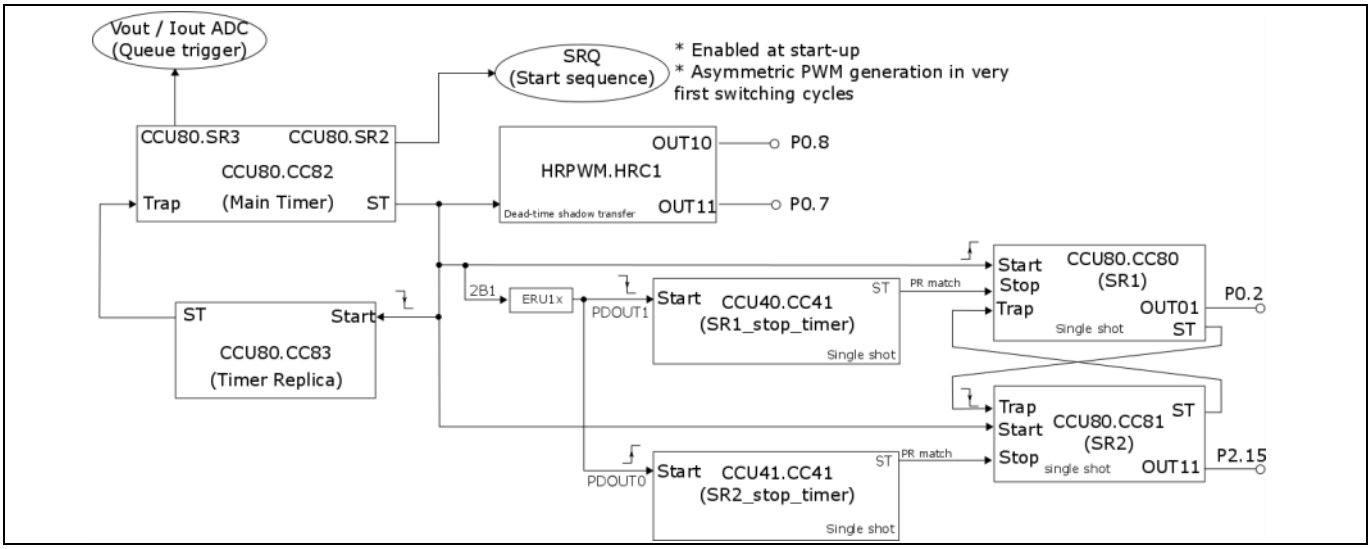

Figure 31 Timer configuration for the LLC of the 800 W power supply

The same main timer information is sent to the SR timers, which are configured in single-shot mode, i.e. the timer counts once to the period every time a start signal arrives. With this information the SR timers are started synchronously with the main timer and the turn-on delay is adjusted by the SW. The turn-off time is controlled by the SW, but an HW limitation linked to the main timer is introduced. In this case, an intermediate timer (SR1/2_stop_timer in Figure 31) is included to take into account the possible delay between primary and secondary signals in the driving scheme. This connection is possible due to the Event Request Unit (ERU) available in the XMC4000 series, which enhances the peripheral connectivity. In addition, the SR timers are configured to trap each other, thus minimizing possible cross-conduction due to asynchronous timing changes motivated by the single-shot behavior. Figure 32 shows a no-load to full-load jump with no drain-source voltage spikes in the 40 V secondary-side OptiMOS™ during the transition, according to the peripheral/SW configuration shown.

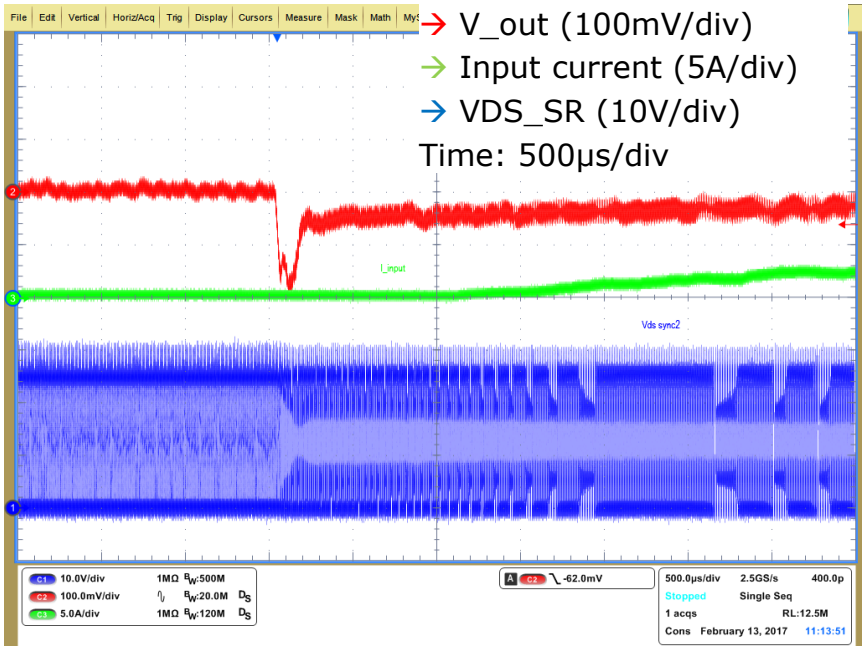

Figure 32 No voltage spikes during the no-load to full-load transition

Under certain operating conditions the LLC half-bridge must be turned off, and this transition must be without voltage or current stress in the converter. Among these conditions, it is possible to find ABM operation or input voltage brownout, as well as remote on/off command.

Again using the main timer as a time base, a timer-replica is generated, and the output signal of this timer is used to trap the main timer (Figure 31). Since the status of the timer replica happens synchronously with the main timer, the primary PWM signal can be turned off synchronously at the end of a switching cycle, and the same happens when the converter operation is resumed, i.e. ABM operation. Figure 33 shows the moment in which the LLC converter is turning off based on an external off signal. As can be seen, no voltage stress is suffered by the SR switch.

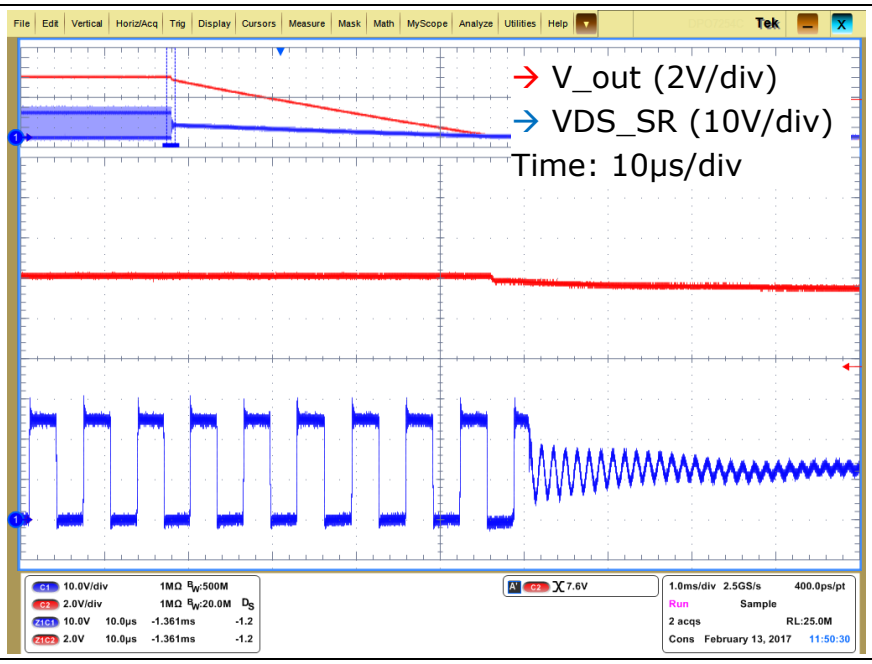

Figure 33 LLC converter turns off synchronously at the end of the switching cycle without voltage stress

4.2.3 Voltage controller and state machine

The control implementation of the LLC converter in the XMC4200 is based on a PID controller which modifies the switching frequency of the converter in order to regulate the output voltage. The controller must be designed to fulfill the output specifications considering the load variation and the wide input voltage range. This is probably the main concern when designing the controller, since the bulk voltage can change from 330 V to 430 V, under any load condition.

Figure 34 shows the voltage controller block diagram, which includes a soft-start path. During soft-start an open-loop linear variation of the switching frequency is applied, i.e. the frequency is linearly decreased toward the minimum allowable frequency. In parallel, the voltage loop (PID controller) is executed with a constant reference, which corresponds to the desired output voltage. The transition from open-loop to closed-loop operation is done either when the output voltage error is under a defined range, or when the closed-loop frequency is higher than the open-loop one.

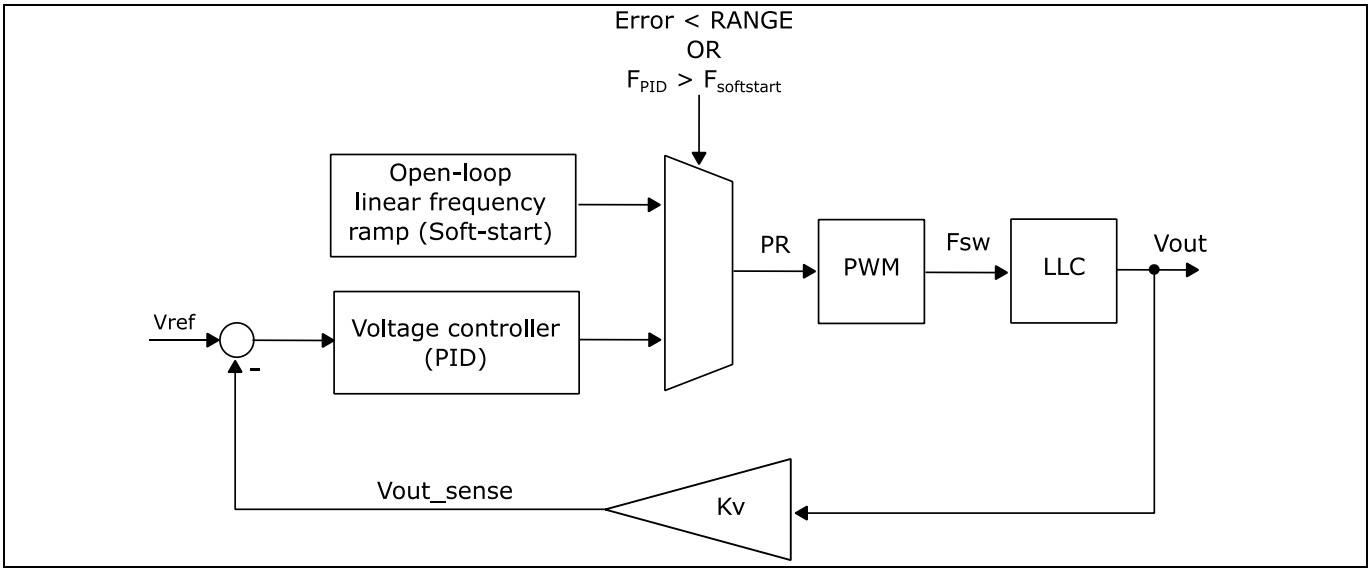

Figure 34 LLC voltage loop diagram block, including soft-start path

The soft-start shown is integrated into a state machine (Figure 35) that controls the different operating conditions of the DC-DC stage in the 800 W server power supply. A part from the start-up sequence and soft-start, the SR management, the ORing switch control, ABM detection and converter restart in case of input and output protections are considered in the state machine. In addition a remote on-off functionality is integrated, according to an external signal that can be managed by a switch incorporated into the load connector board (Figure 6).

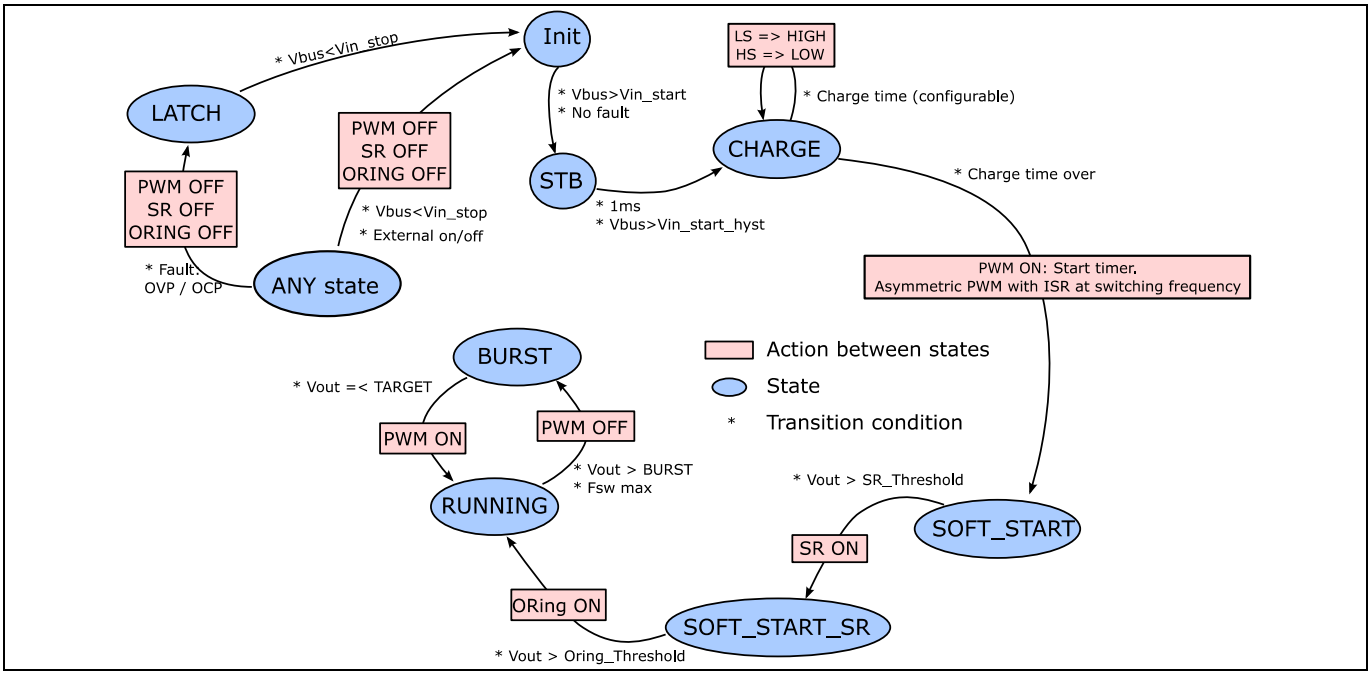

Figure 35 LLC state machine

Figure 36 shows the output voltage variation during start-up when the state machine shown in Figure 35 is applied, which includes the soft-start architecture shown above. During this process, the output voltage is monitored in order to decide when the SR switches should be turned on (in the beginning they behave as diodes) as well as the point at which the ORing switch is closed. Both decisions are taken when the output voltages reach 10 V and 11.5 V respectively, as marked in Figure 36.

Note: No special function is applied for the ORing switch, since the implemented SW is not intended for hot plug or parallel operation.

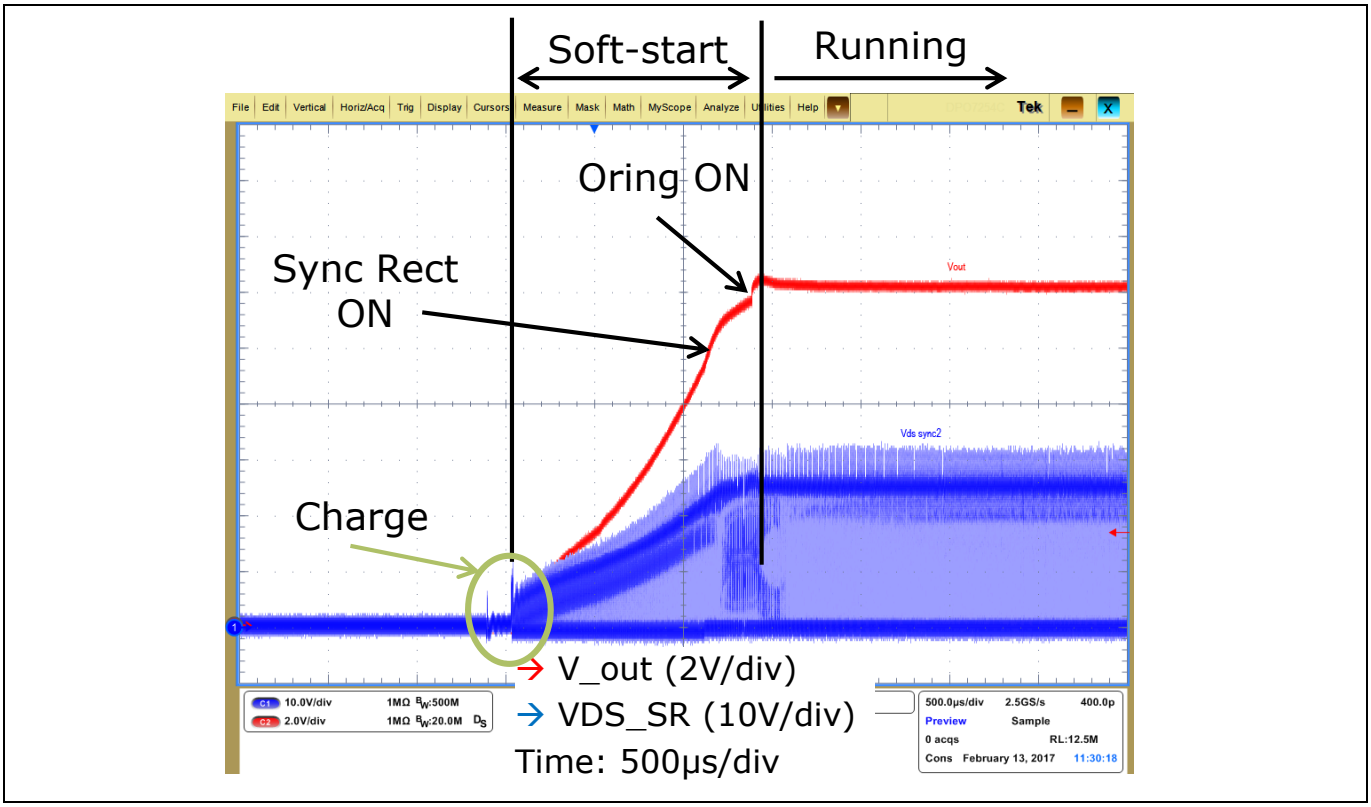

Figure 36 Output voltage during the start-up of the LLC of the 800 W server power supply

The implemented driving scheme in the LLC converter of the 800 W power supply is based on a level shifter with bootstrap capacitor. This capacitor must be charged before the PWM starts in order to achieve proper operation of the converter.

Therefore, before the previously described soft-start sequence starts, a long pulse is applied to the low-side switch of the LLC half-bridge. This pulse can be seen in the blue waveform of Figure 37, which shows the PWM and ORing signals during the start-up. In the detail view of the same figure, it can be appreciated how the PWM operation starts after this long pulse. A short time with both half-bridge signals in the low level is introduced between the long pulse and the PWM operation to avoid half-bridge shoot-through.

In steady-state operation, the LLC converter is controlled by modifying the switching frequency of a 50% PWM. However, the applied starting pulse to charge the bootstrap capacitor provokes a voltage imbalance in the resonant capacitors. This imbalance can trigger hard-commutation situations if the resonant current is not allowed to change polarity before the active half-bridge switch is changed. To avoid this situation a PWM with a duty cycle other than 50% is applied, until the resonant capacitors are properly balanced, as shown in the detail view of Figure 37. At that point, the soft-start process described above begins.

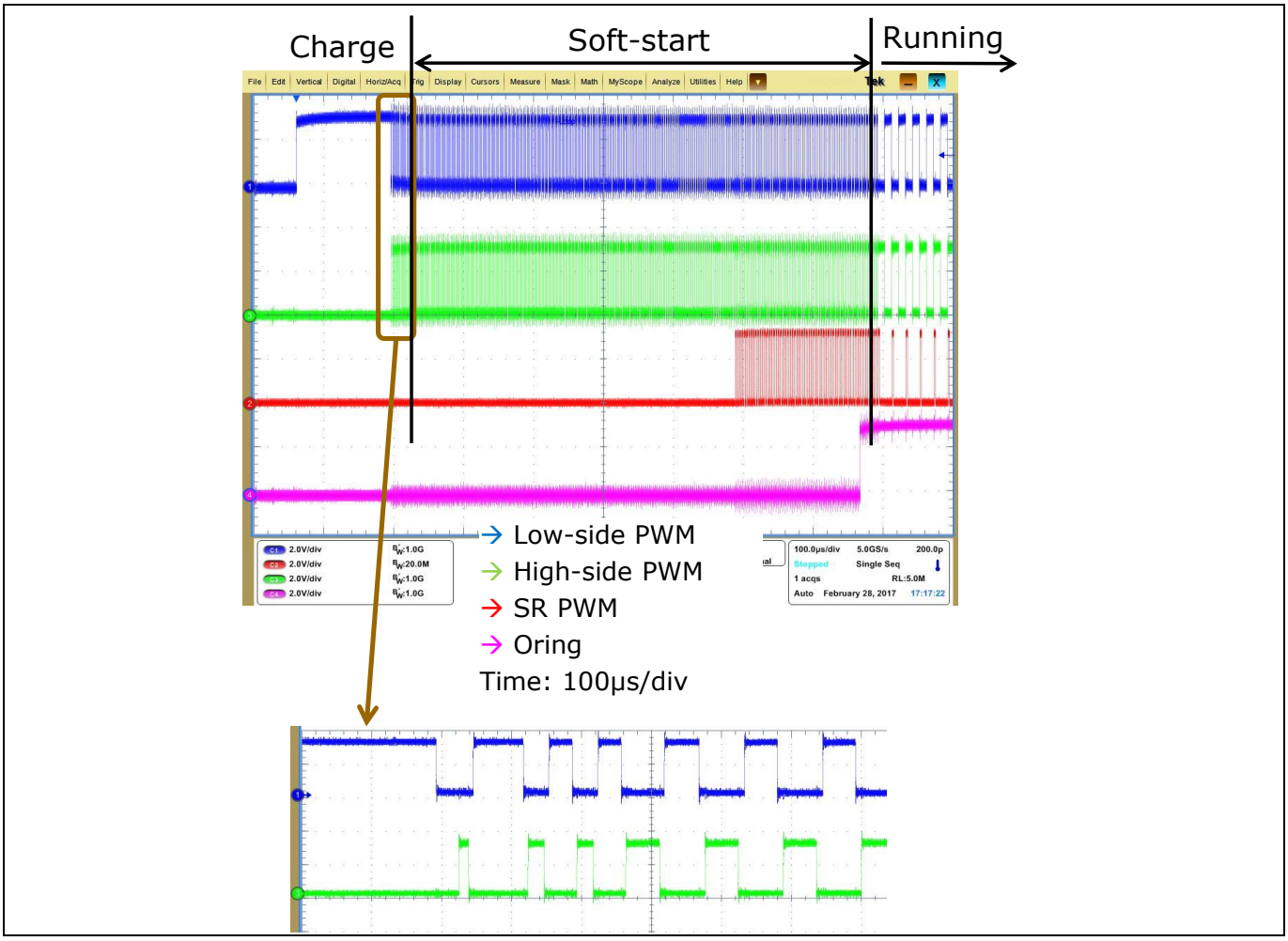

Figure 37 Half-bridge (low-side and high-side) and SR PWM signals and ORing signal during start-up; the bottom diagram is a detail view of the first half-bridge PWM pulses

ABM operation is enabled when the applied switching frequency is maximum, and the output voltage is over a specified offset (150 mV).

4.2.4 Protections and fan management

The LLC implements input and output protections as well as temperature protection and fan management.

As already described, the input voltage (bulk voltage) is sensed by the primary-side controller and received by the LLC controller via UART. The received value is used for the brownout protection: the converter is started when the bulk voltage reaches 390 V and is turned off if the received voltage is under 330 V.

Regarding the output, both current and voltage protections have been included. In respect to the OVP, the LLC converter turns off if the output voltage reaches 14 V. The bulk voltage must go under 330 V (brownout) for the LLC converter to restart.

The OCP is divided into three different levels, with different times allowed for a given OC, as shown in Figure 38. The OCP is enabled after the soft-start phase in the state machine. As in the OVP case, a brownout is necessary for the LLC to restart after an OCP trigger.

An extra current protection is implemented based on the resonant current measurement, as introduced in section 4.2.1. This protection is meant to be a fast, HW implemented protection in case of short-circuit operation.

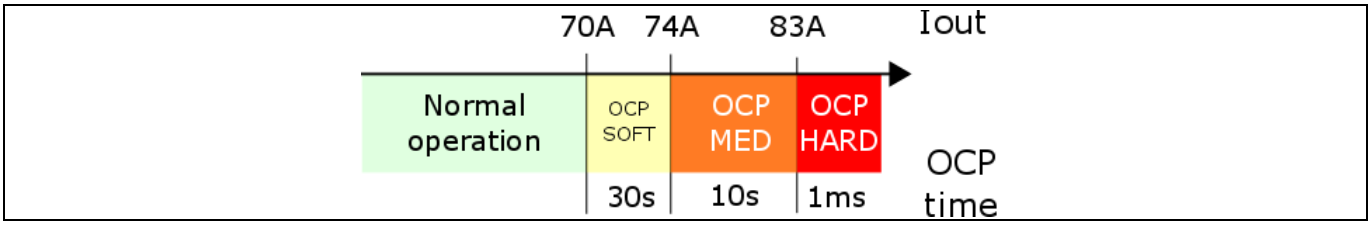

Figure 38 OCP levels with the time limit established for each of them

Similar to the input voltage information, the temperature information is sent by the primary-side controller (XMC1402) via UART and the digital isolator. The heatsink temperature is acquired in the primary controller by means of a voltage partition, which includes a Negative Temperature Coefficient (NTC) thermistor. The received information is used to modify the duty cycle of the PWM applied to the fan, i.e. the speed of the fan, according to the graph shown in Figure 39.

The temperature information is also used for over-temperature protection. In this case, if the received temperature is over 120°C the LLC converter is turned off. The PFC converter maintains no-load operation with regulated bulk voltage. The DC-DC stage is restarted if the heatsink temperature drops under 100°C.

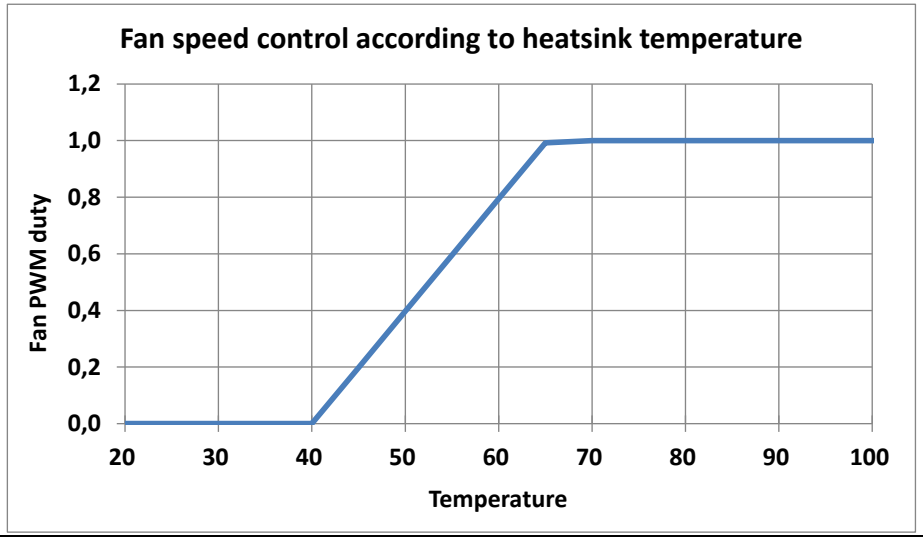

Figure 39 Fan speed variation with respect to the heatsink temperature

5 Auxiliary converter

The auxiliary power supply provides the required bias supplies for the control and driving circuitry of both primary and secondary converters. The auxiliary converter has been specifically designed for the 800 W server power supply using the flyback QR controller ICE2QR2280G CoolSET™. In this case a Surface Mounted (SM) version is utilized to fit into the power supply form factor, since the bias converter is implemented directly on the main board.

It must be noted that no output of the auxiliary supply is available in the output connector, but all the generated supplies are used internally in the server power supply. The fan is supplied directly from the LLC output voltage, rather than via an extra winding in the auxiliary power supply. Efficiency is the reason for this configuration, since the necessary 3.3 W to drive the fan at maximum speed would be processed with around 80% efficiency in the auxiliary power supply, against the achievable 96% for the same power in the LLC converter.

The auxiliary converter concept is shown in Figure 40. The XMC4200 voltage supply (3.3 V_sec) is directly regulated and the rest of the supplies are generated accordingly by using the adequate turn ratio. The primary-side controller supply voltage (3.3 V_pri) is generated from a 13 V winding using the integrated buck converter IFX91041EJV33.

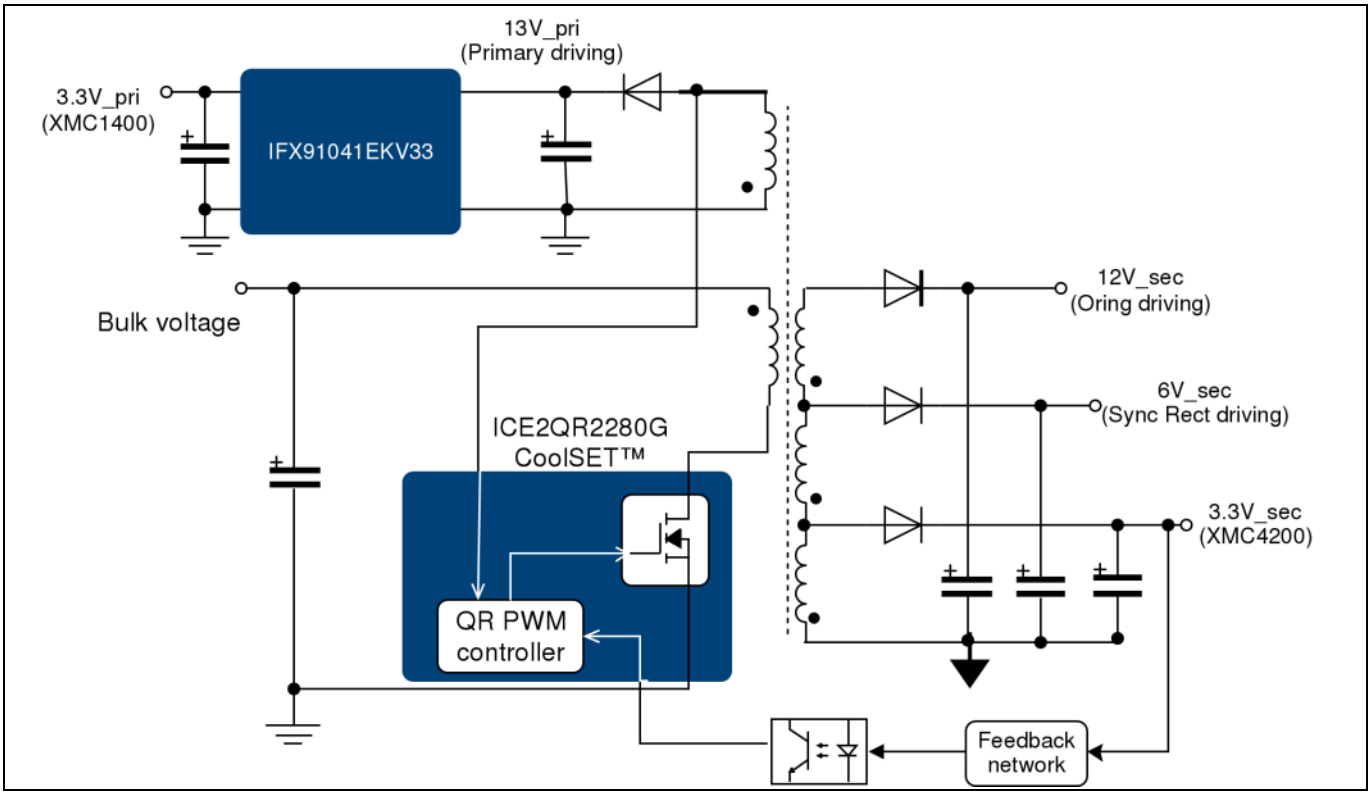

Figure 40 Block diagram with the required supplies for the 800 W server PSU

6 Test results

This chapter introduces the performance and behavior of the 800 W server power supply with CoolMOS™ C7. Table 4 shows a summary of the tests described in this section.

Table 4 Summary of the tests described in this section with the applied conditions and the main results

Test		Conditions	Result	
Efficiency test		230 V_{rms} 50 Hz, 10% to 100% load	η_{pk} = 95.32% at 400 W; > 1% over 80Plus® Platinum® efficiency	
		115 V_{rms} 60 Hz, 10% to 100% load	η_{pk} = 93.95% at 322 W	
		90 V_{rms} 60 Hz, 10% to 100% load	η_{pk} = 92.99% at 322 W	
Current THD		230 V_{rms} 50 Hz, 10% to 100% load	THDi < 10% from 20% load	THDi ≈ 2% at 100% load
		115 V_{rms} 60 Hz, 10% to 100% load	THDi < 6.5% from 10% load	
		90 V_{rms} 60 Hz, 10% to 100% load	THDi < 4% from 10% load	
PF		230 V_{rms} 50 Hz, 10% to 100% load	PF > 0.9 from 20% load	
		115/90 V_{rms} 60 Hz, 10% to 100% load	PF > 0.96 from 10% load	
Steady-state V_{out} ripple		230/115/90 V_{rms} 50/60 Hz, 10% to 100% load	$\lvert\Delta V_{out}\rvert$ < 120 mVpk-pk	
Inrush current		230 V_{rms}, 50 Hz	Iin_peak < 10 A	
PLD	AC lost	200/100 V_{rms} 50/60 Hz AC lost: 10 ms at 100% load, 20 ms at 50% load	$\lvert\Delta V_{out}\rvert$ < 240 mVpk	No damage: * PSU soft-start if bulk voltage under 320 V * PSU soft-start if V AC out of range for certain time
	Voltage sag	200/100 V_{rms} 50/60 Hz Different sag conditions; 100% load		
Brownout		100 V → 60 V, 60 Hz, 40 s – 40 steps	82 V OFF	
		60 V → 100 V, 60 Hz, 40 s – 40 steps	86 V ON	
Load transient		3 A ↔ 33 A, 0.5 A/µs	$\lvert\Delta V_{out}\rvert$ < 240 mVpk	
		33 A ↔ 66 A, 0.5 A/µs		
		33 A → 0 A	ΔV_{out} < 200 mV (ABM operation)	
OCP		30 s at 72 A	LLC OFF Resumption of operation requires bulk voltage to drop under 320 V	
		10 s at 78 A		
		100 A		
		Output terminals in short-circuit	Detection within 100 µs; LLC OFF Resumption of operation requires controller reset	
EMI		230 V_{rms} 50 Hz, full-load, resistive load, lab set-up	Complies with class B limits	

6.1 Performance and steady-state operation

This section describes the steady-state waveforms of the server PSU under different operating conditions. In addition, the PSU efficiency, THD and PF are shown.

Table 5 shows the efficiency measurements obtained from the 800 W server power supply for different input voltages and from 10% of the load to full-load operation. The same data is plotted in Figure 41. It can be concluded that the server power supply shown is far over the Platinum® standard efficiency limit. As an example, the efficiency at half-load and high-line (230 Vrms) is 1.3% over the mentioned limit. The efficiency measurements shown do not include the fan supply, which was externally powered.

Table 5 Measured efficiency of the 800 W server power supply

Output current (A)	Eff. (%) at 230 V_{rms}	Eff. (%) at 115 V_{rms}	Eff. (%) at 90 V_{rms}
6.6	90.03	89.19	88.32
13.2	93.76	92.57	92.2
19.8	94.79	93.62	92.9
26.4	95.26	93.95	92.99
33	95.32	93.86	92.72
39.6	95.27	93.58	92.25
46.2	95.15	93.24	91.68
52.8	94.97	92.83	91.02
59.4	94.74	92.37	90.21
66	94.47	91.79	89.15

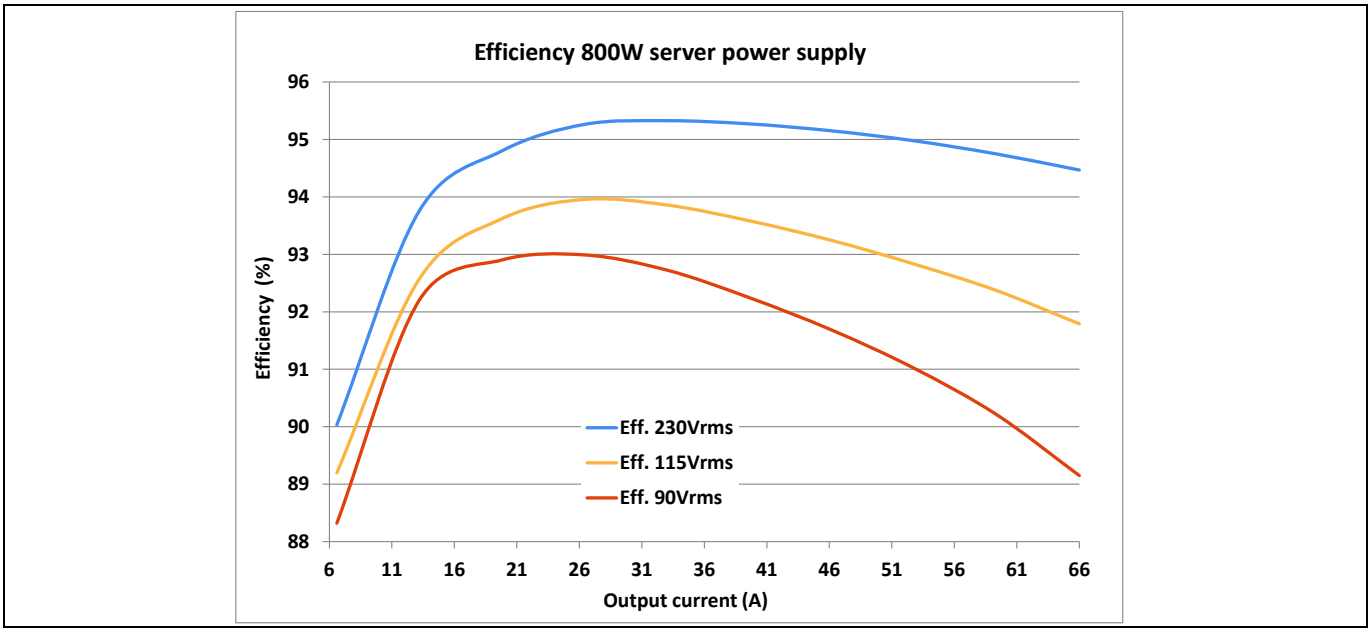

Figure 41 Measured efficiency of the 800 W server power supply

The input current quality, in terms of THD and PF, is shown in Table 6 and Table 7 respectively. This information is graphically presented in Figure 42 and Figure 43 as well. For low-line operation (90 V_{rms} and 115 V_{rms} at 60 Hz) the THD is under 7% for the whole tested range, with a PF over 0.95. On the other side, for high-

line (230 V_{rms} at 50 Hz) the THD is under 10% from 20% of the load onward, with a PFC over 0.9 from the same load conditions up to full-load, as specified in section 2.1.

Table 6 Measured input current THD of the 800 W server power supply

Output current (A)	THD (%) at 230 V_{rms}	THD (%) at 115 V_{rms}	THD (%) at 90 V_{rms}
6.6	15.35	6.51	4.06
13.2	9.91	2.8	2.24
19.8	8.48	2.04	2.04
26.4	6.51	1.83	1.79
33	3.9	1.66	1.79
39.6	2.35	1.78	1.78
46.2	1.82	1.89	1.87
52.8	1.63	2.01	1.84
59.4	1.5	1.93	1.92
66	1.41	2	2.13

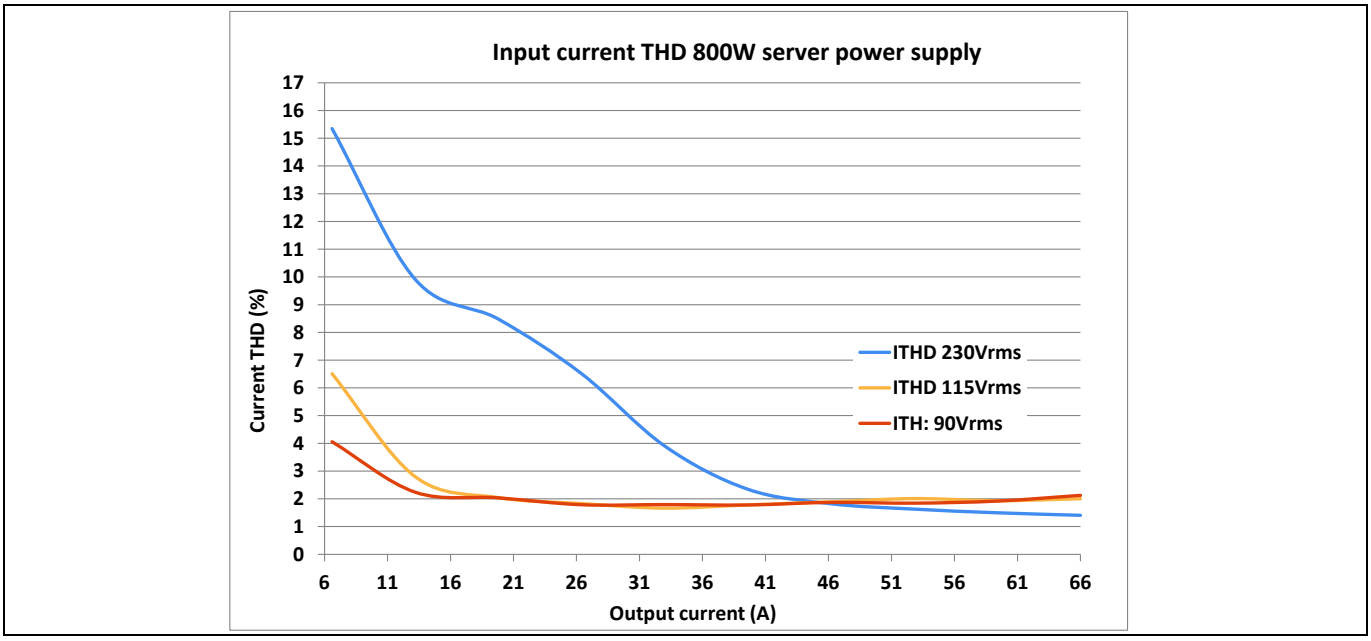

Figure 42 Measured THD of the 800 W server power supply

Table 7 Measured PF of the 800 W server power supply

Output current (A)	PF at 230 V_{rms}	PF at 115 V_{rms}	PF at 90 V_{rms}
6.6	0.774	0.966	0.984
13.2	0.902	0.989	0.997
19.8	.945	0.997	0.999
26.4	0.964	0.998	0.999
33	0.972	0.999	0.999
39.6	0.981	0.999	0.999
46.2	0.987	0.999	0.999

Output current (A)	PF at 230 V_{rms}	PF at 115 V_{rms}	PF at 90 V_{rms}
52.8	0.991	0.999	0.998
59.4	0.994	0.999	0.998
66	0.995	0.999	0.998

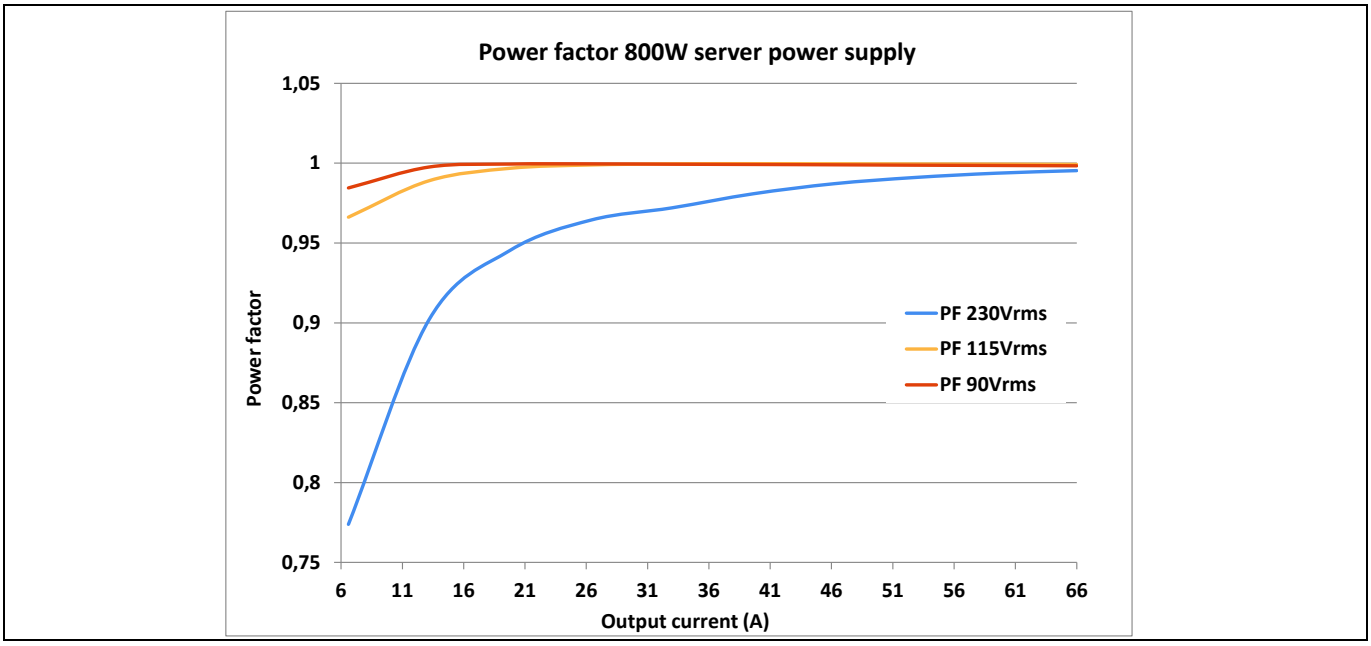

Figure 43 Measured PF of the 800 W server power supply

The steady-state waveforms of the PSU for both high-line and low-line are shown in Figure 44 and Figure 45 respectively, for 20% and full-load operation. It can be seen how the input current degrades in light load at high-line because of the DCM operation referred to previously. Regarding the output voltage, the peak-to-peak ripple is inside the specified ±120 mV. The Bulk Voltage Modulation (BVM) can be also seen in the waveforms shown. In the case of 20% load a 395 V bulk voltage is measured, while this value increases to 405 V in the case of full-load operation.

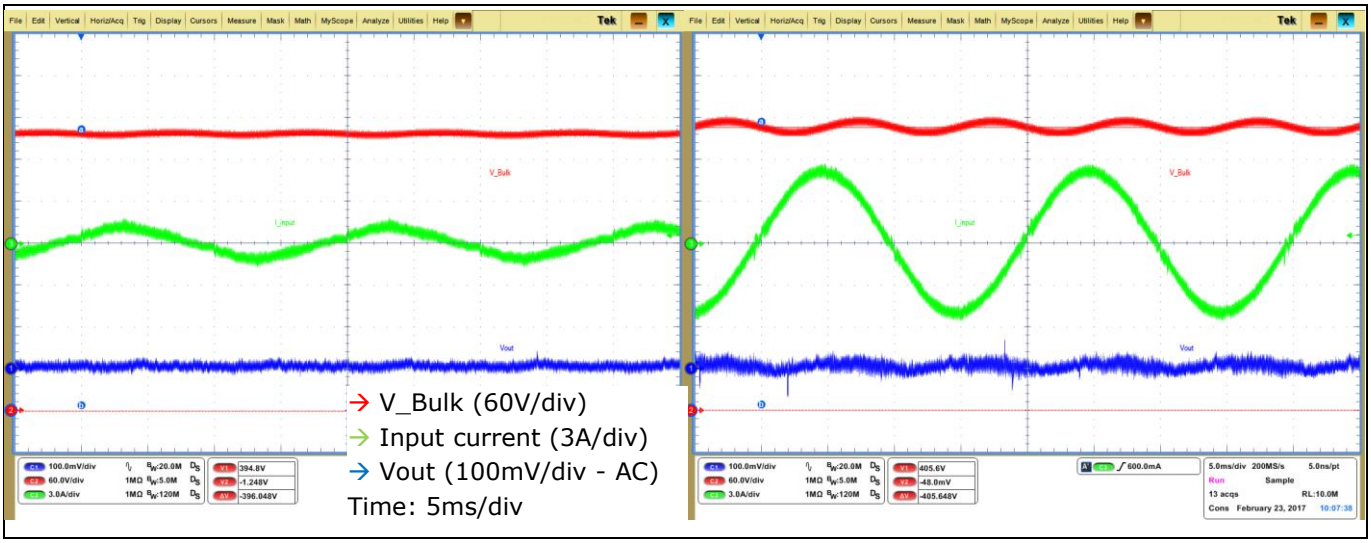

Figure 44 Input current, bulk voltage and output voltage for the 800 W PSU at 20% (left) and 100% (right) load, 230 V_{rms} 50 Hz operation

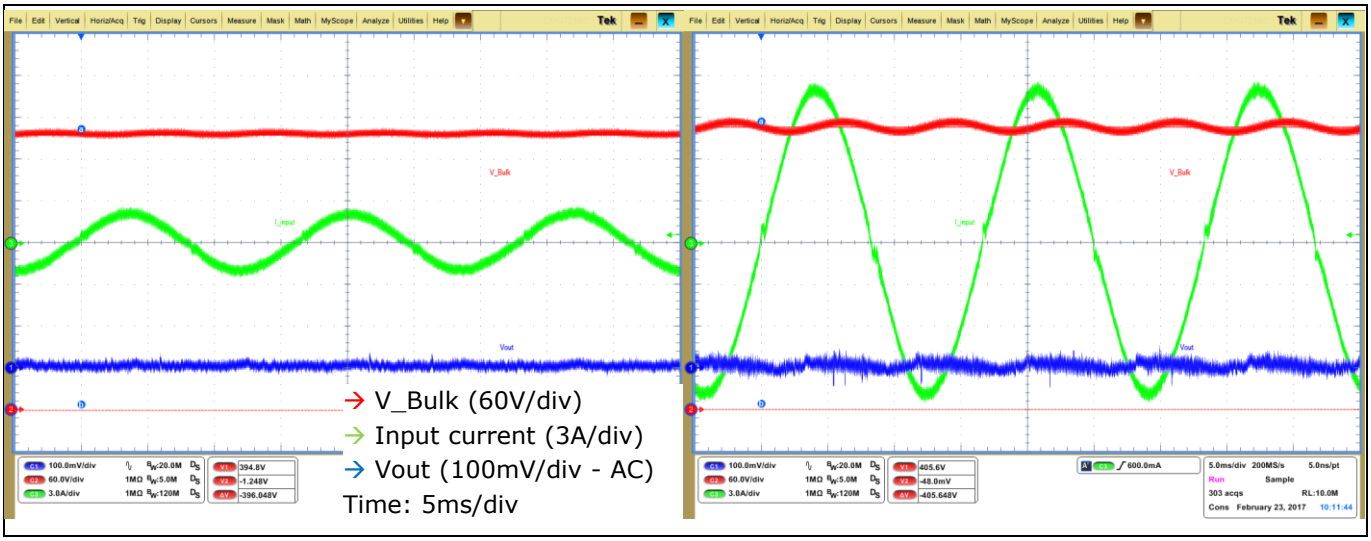

Figure 45 Input current, bulk voltage and output voltage for the 800 W PSU at 20% and 100% load, 115 V_{rms} 60 Hz operation

6.2 Inrush current (waveforms)

The power supply start-up at high-line and full-load is shown in Figure 46. Due to the implemented state machine in both PFC and LLC, a time is required for the start-up of both converters after the input and bulk voltages are detected as being within the proper values. The inrush current in these conditions is shown in detail in Figure 47. As can be seen, the inclusion of an NTC resistor in the PFC input limits the inrush current to under 10 A in the tested conditions.

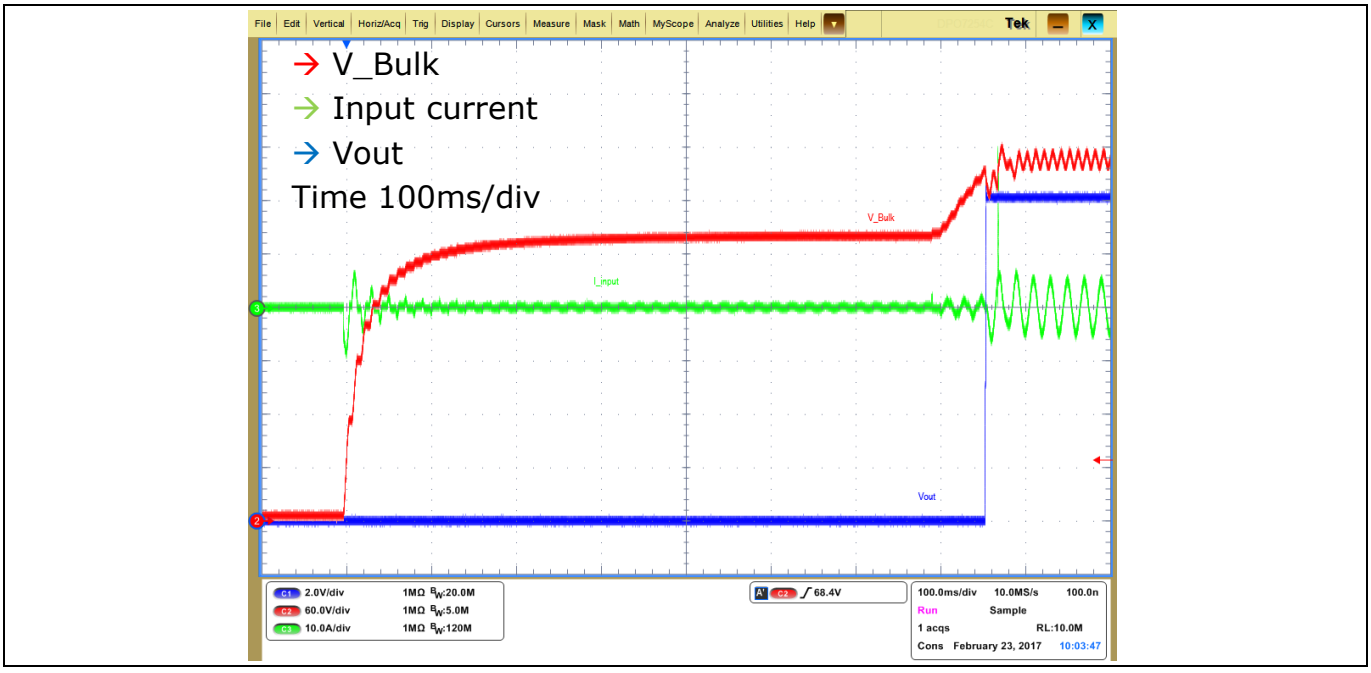

Figure 46 PSU start-up at 230 V_{rms} and full-load

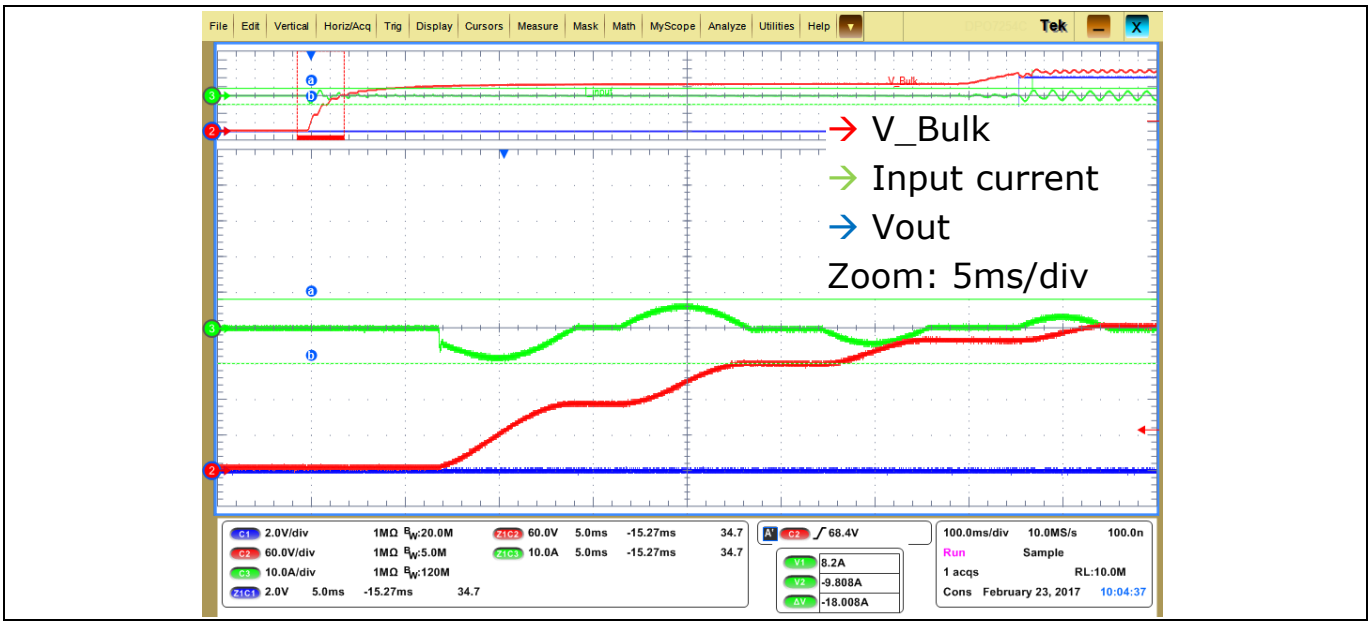

Figure 47 Detail of the PSU inrush current during start-up at 230 V_{rms} and full-load

6.3 Power Line Disturbance (PLD)

Different PLDs can appear when connected to the grid. These conditions have been tested using a programmable AC source. In this section, the PLD conditions are separated into AC lost during half-cycle, known as ACLDO, and voltage sags. The results shown are obtained for full-load operation.

The applied conditions for the ACLDO test are summarized in Table 8. The AC is removed during 10 ms in a 100 ms period and this loss is run 10 consecutive times, for both low- and high-line. The unit must operate error-free, i.e. output voltage must remain inside the defined dynamic limits, in the case of ACLDO. In the tests described, an angle of 45 degrees is used for the ACLDO synchronization, since it shows the worst point from the bulk voltage point of view.

Table 8 Applied voltages and cycles for the ACLDO test

		1st to 10th time	
Duty cycle	Initial 5–10 s	10% (10 ms)	90% (90 ms)
AC input	100 V AC	0 V AC	100 V AC
	200 V AC	0 V AC	200 V AC

The results of the applied test are shown in Figure 48 and Figure 49 for 100 V_{rms} input, and in Figure 50 and Figure 51 when 200 Vrms are applied as AC voltage. In both cases, the bulk voltage decreases to 340 V during the AC loss and a fast response of the bulk voltage is observed, since maximum current is applied until the bulk voltage reaches 385 V. This extra injected current takes the bulk voltage to over-shoot, despite the enhanced BW of the implemented voltage loop. In that case the PFC is turned off until the bulk decreases to the regulation level. This bulk voltage variation implies a certain ripple in the output voltage. In any case the dynamic range of the output voltage is under the specified 2%.

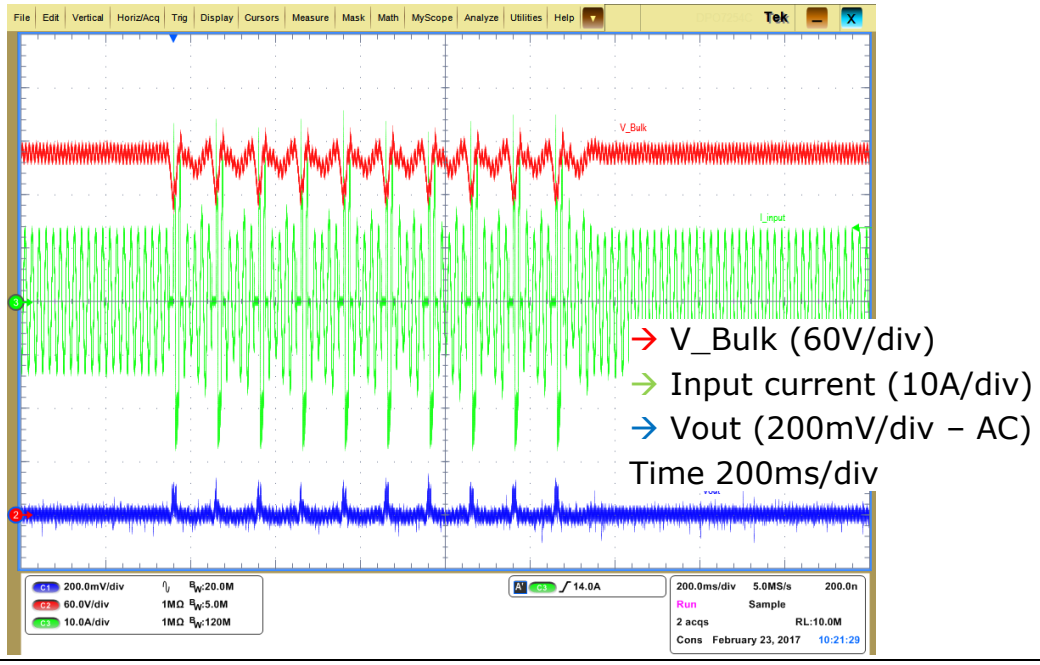

Figure 48 800 W PSU response to 10 times ACLDO at 100 V and 45 degrees, as defined in Table 8

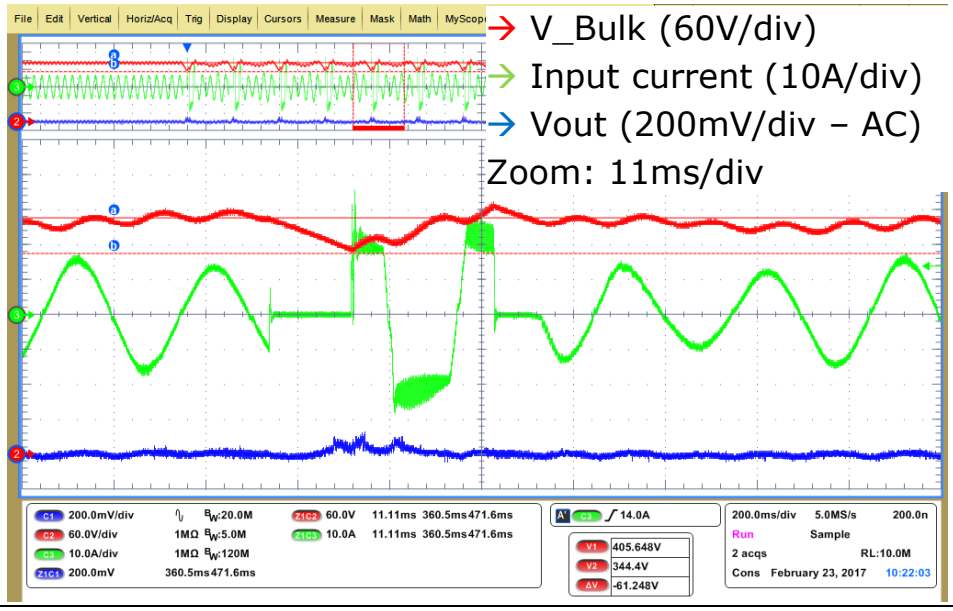

Figure 49 Detail of the response to 10 times ACLDO at 100 V and 45 degrees, as defined in Table 8

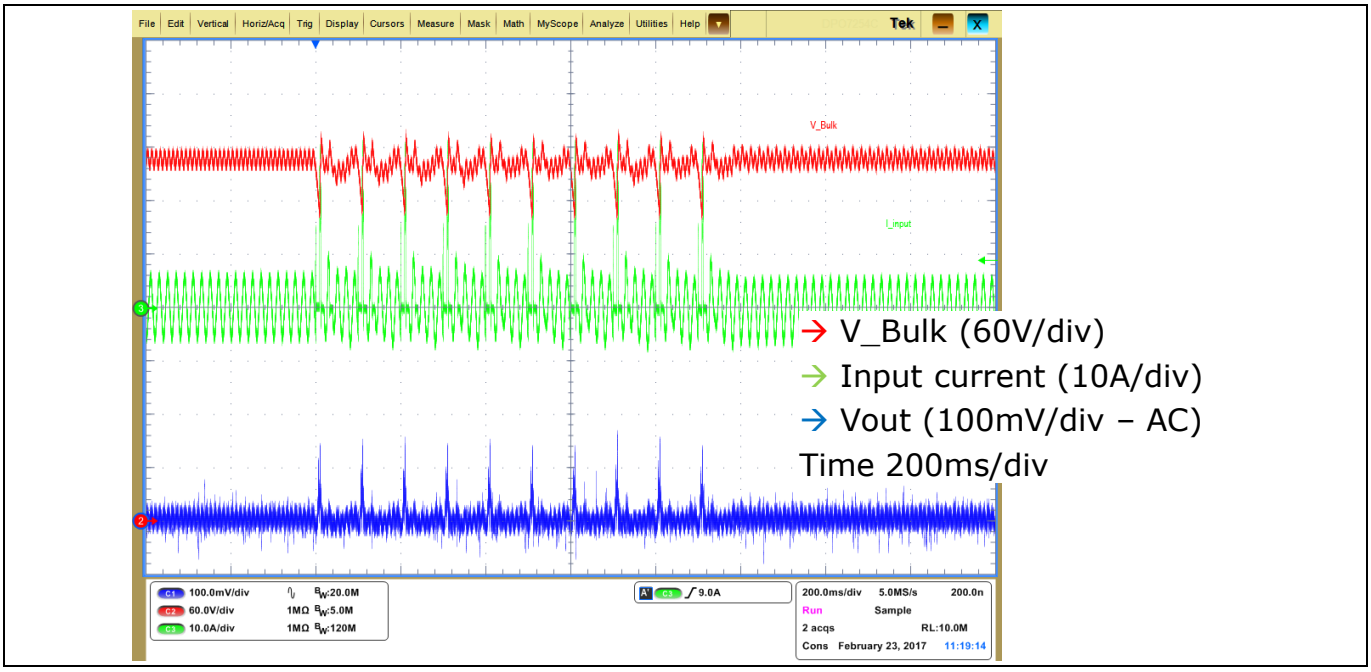

Figure 50 800 W PSU response to 10 times ACLDO at 200 V and 45 degrees, as defined in Table 8

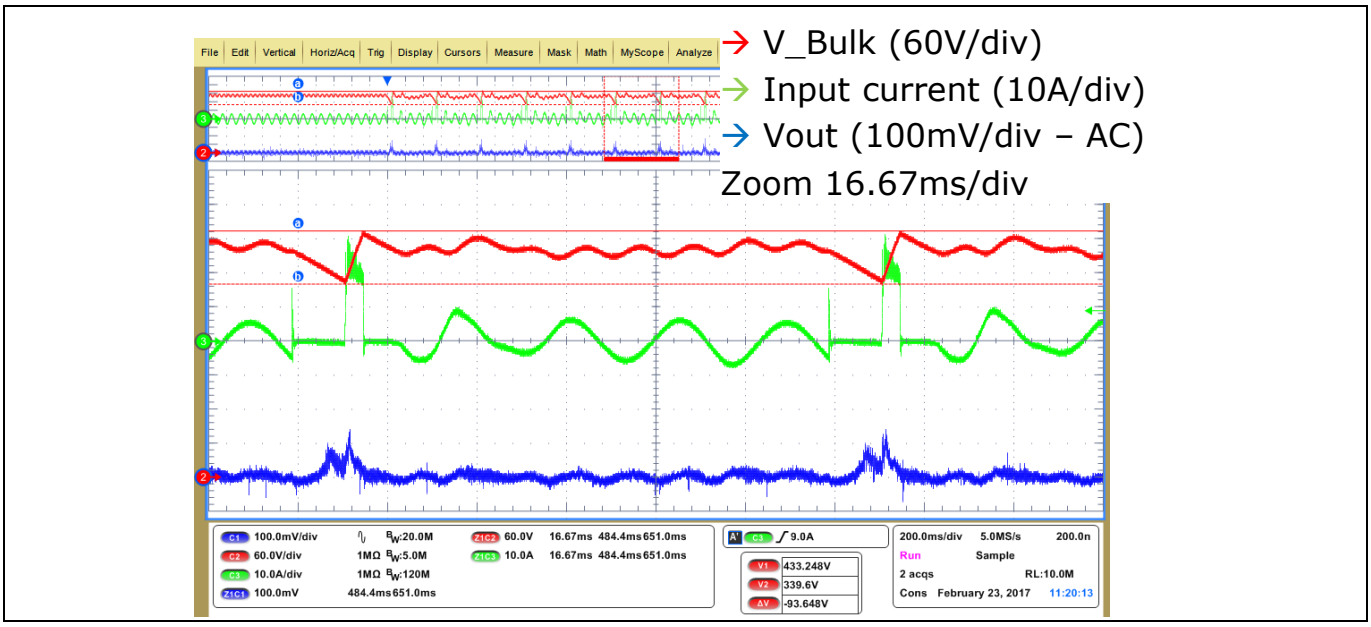

Figure 51 Detail of the 800 W PSU response to 10 times ACLDO at 200 V and 45 degrees, as defined in Table 8

If the loss of AC voltage lasts for more than 10 ms and the bulk voltage decreases under 333 V, both the PFC and LLC stages are turned off and a soft-start of the system is initiated. Figure 52 shows the system behavior when the AC is removed for 15 ms for full-load operation. The bulk voltage decreases to 332 V and therefore the PSU turns off. After a defined time of 100 ms, the start-up process stars with the PFC and LLC soft-start.

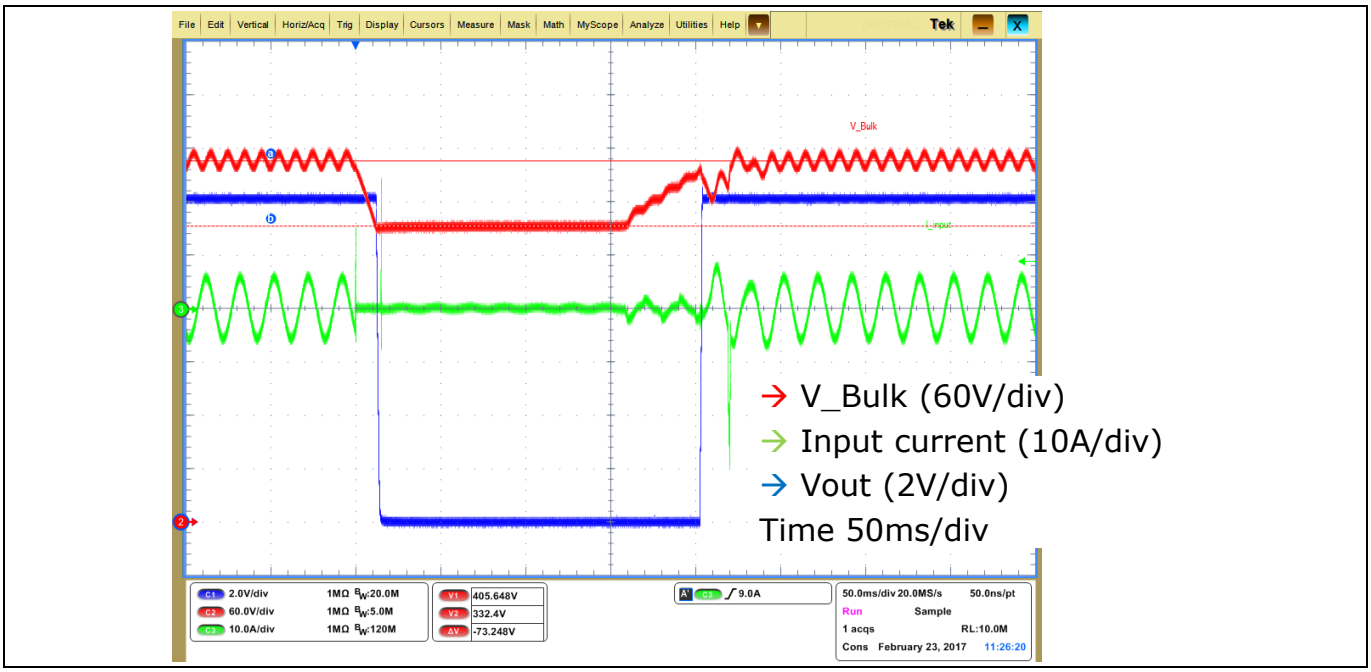

Figure 52 800 W PSU response to 15 ms ACLDO at 200 V and 45 degrees for full-load conditions

A second PLD condition is voltage sag, which is a temporary decrease in the line voltage. Table 9 shows the two different voltage stages tested in the 800 W PSU, including the timing applied. In this section the results for low-line (100 V) are shown, since the voltage reduction from 200 V to either 130 V or 150 V is inside the steady-state specifications.

Table 9 Applied voltages and cycles for voltage sag test

		1st to 10th time	
Duty cycle	Initial 5–10 s	10% (0.5 s)	90% (4.5 s)
AC input	100 V AC	68 V AC	100 V AC
	200 V AC	130 V AC	200 V AC

		1st to 10th time	
Duty cycle	Initial 5–10 s	10% (2 s)	90% (18 s)
AC input	100 V AC	75 V AC	100 V AC
	200 V AC	150 V AC	200 V AC

The result of the 68 V voltage sag applied during 500 ms with a period of 5 s is shown in Figure 53 for two consecutive variations. Figure 54 gives an insight into the waveforms at the beginning of the voltage sag. The system response when 75 V are applied during 2 s with a steady-state voltage of 100 V is shown in Figure 55. A detailed view of the 100 V to 75 V step is shown in Figure 56. All the scope captures shown are taken under full-load conditions.

In both cases the input voltage step makes the PFC reach maximum current limitation, which is set to 20 A, leading to BVM. After this modulation ends, the bulk voltage returns to the expected regulation value (405 V at full-load). The output voltage is not affected by the BVM, since the voltage change is slower than in the ACLDO case.

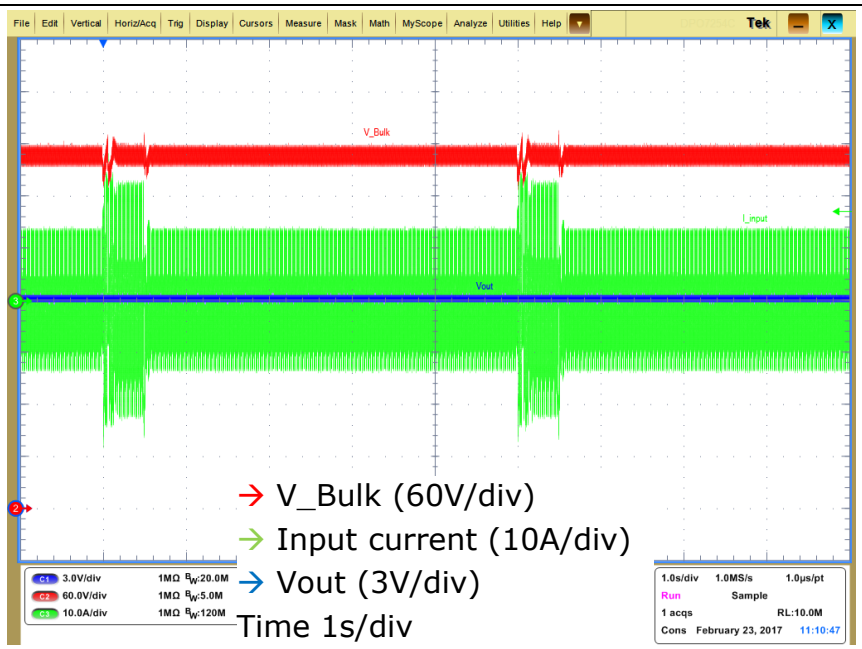

Figure 53 Two-times 68 V voltage sag, as defined in Table 9

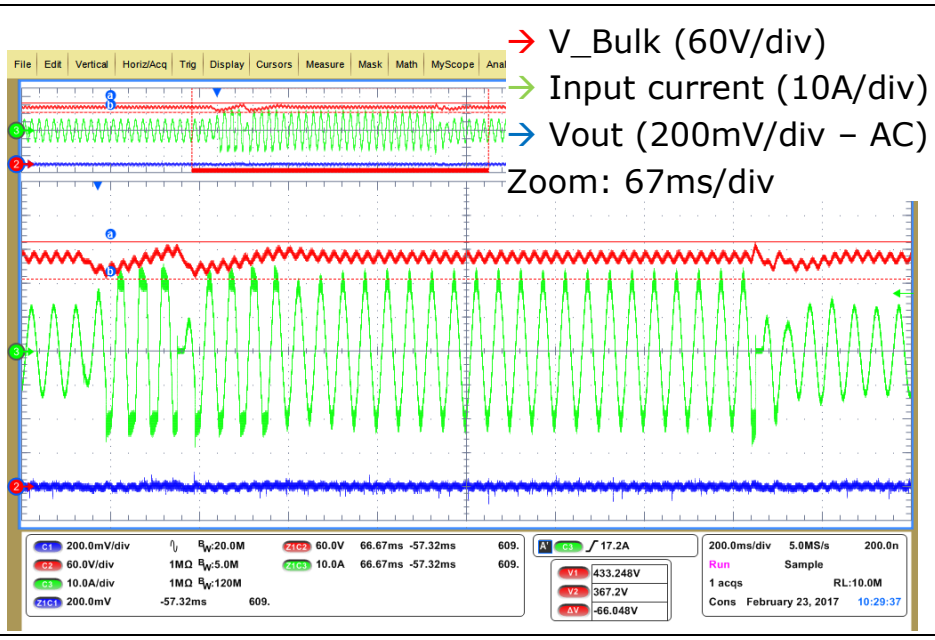

Figure 54 Bulk voltage variation during 68 V sag during 500 ms

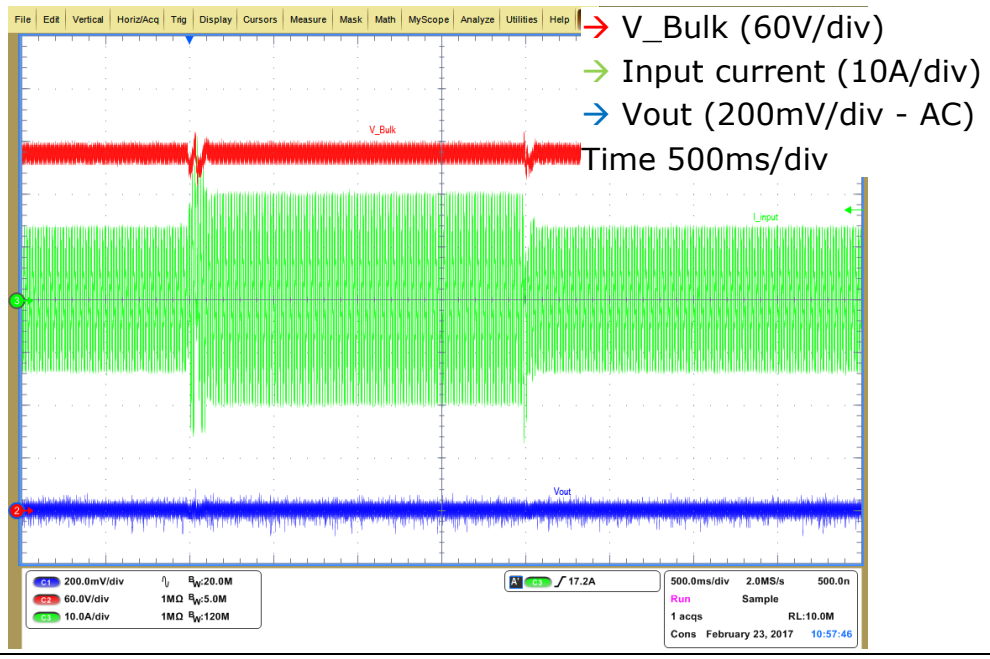

Figure 55 Bulk voltage variation during 75 V sag during 2 s, as defined in Table 9

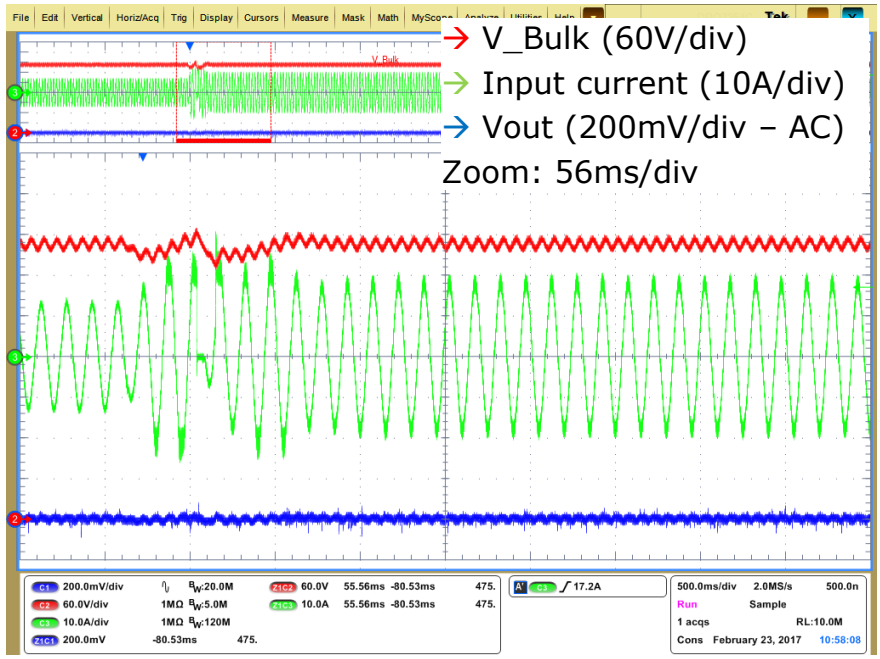

Figure 56 Detail of the 75 V sag during 2 s, input voltage change from 100 Vrms to 75 Vrms

Since the voltage sag shown can be under the brownout levels for steady-state operation, a time filter is implemented in the PFC SW. In case the input voltage is under 82 V for longer than 2 s, or under 75 V for more than 500 ms, the PFC (and therefore the LLC) is turned off. This situation is shown in Figure 57, where 68 V have been applied for 800 ms. The system is turned off and a start-up sequence including soft-start is implemented after the defined 100 ms waiting time.

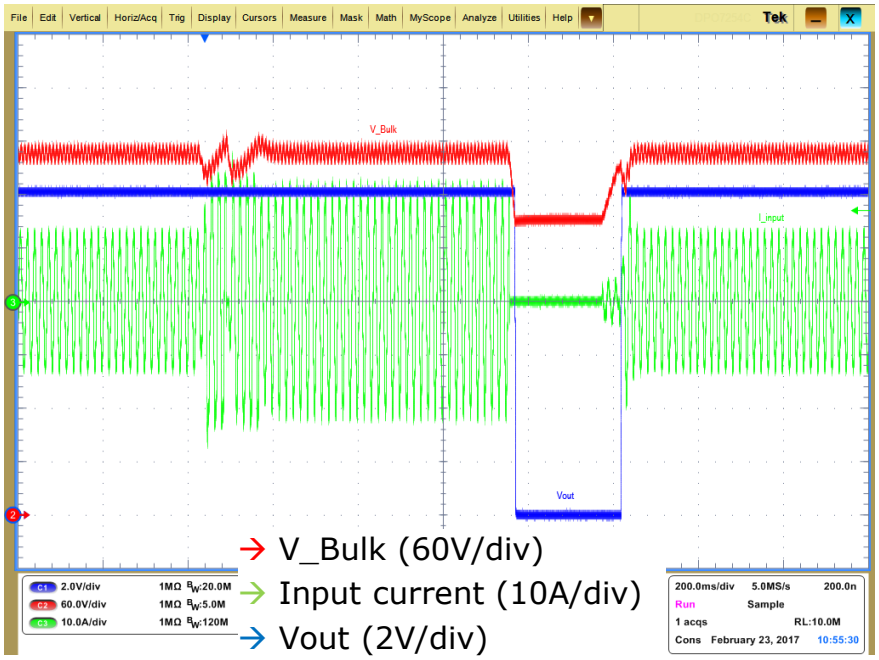

Figure 57 **68 V voltage sag applied for more than 500 ms (800 ms), PFC and LLC turn off and resume operation with soft-start**

6.4 Brownout (graph)

The 800 W server power supply will shut down when the input voltage is under 82 V. The PFC unit implements the time filters introduced in the previous section, which enable managing of the line voltage sag. The unit restarts when the input voltage is higher than 86 V.

Figure 58 shows the brownout behavior at half-load of the power supply, when the input voltage is linearly decreased from 100 V to 60 V, at 60 Hz, during 40 s in 40 steps. Afterwards, the input voltage is increased from 60 V to 100 V, at 60 Hz, linearly with the same slew rate. The unit shuts down with 80 V input and restarts operation at 86 V respectively.

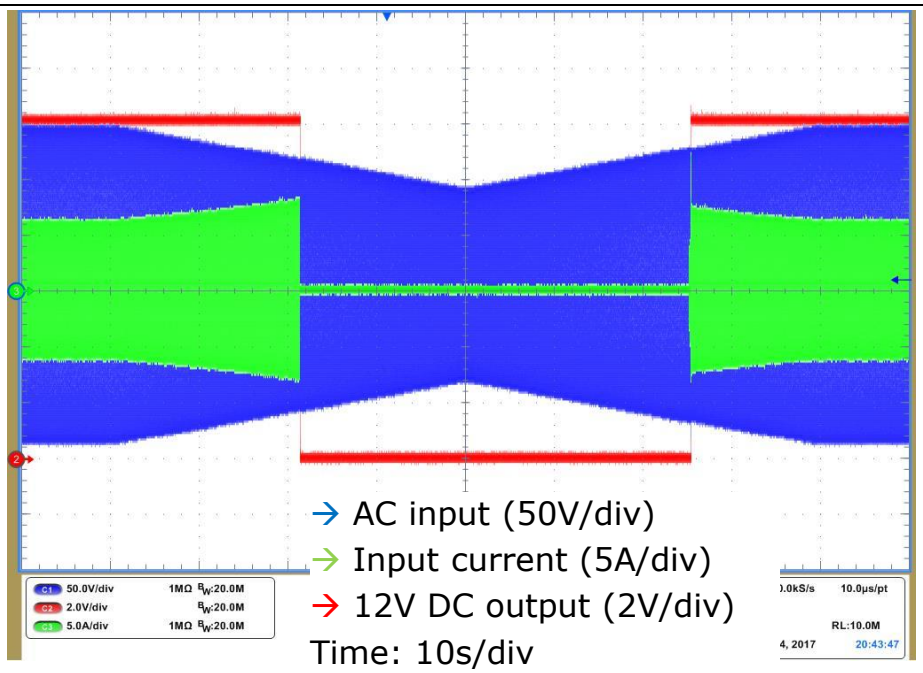

Figure 58 Brownout test with variation from 100 V to 60 V AC during 40 s in 40 steps

6.5 Load transient response (waveforms)

The specification described in section 2.1 establishes a ±2% variation, i.e. ±240 mV, of the output voltage in case of dynamic load-jumps. The specified slope is 0.5 A/µs when the load changes from 3 A (5% load) to 33 A (50% load) and from 33 A to 66 A (100% load), and vice-versa. Figure 59 and Figure 60 show the result of the introduced dynamic test. As can be seen, the 800 W PSU stays within the margins when such load-jumps are applied, with a maximum under-shoot of -182 mV and an over-shoot of approximately 150 mV.

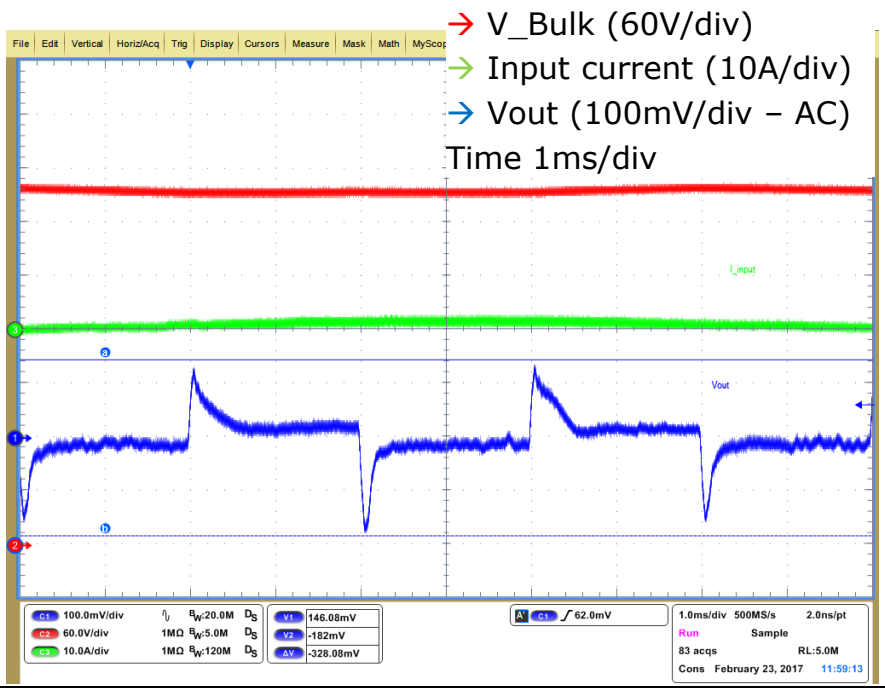

Figure 59 Load-step response 3–33 A at 0.5 A/µs

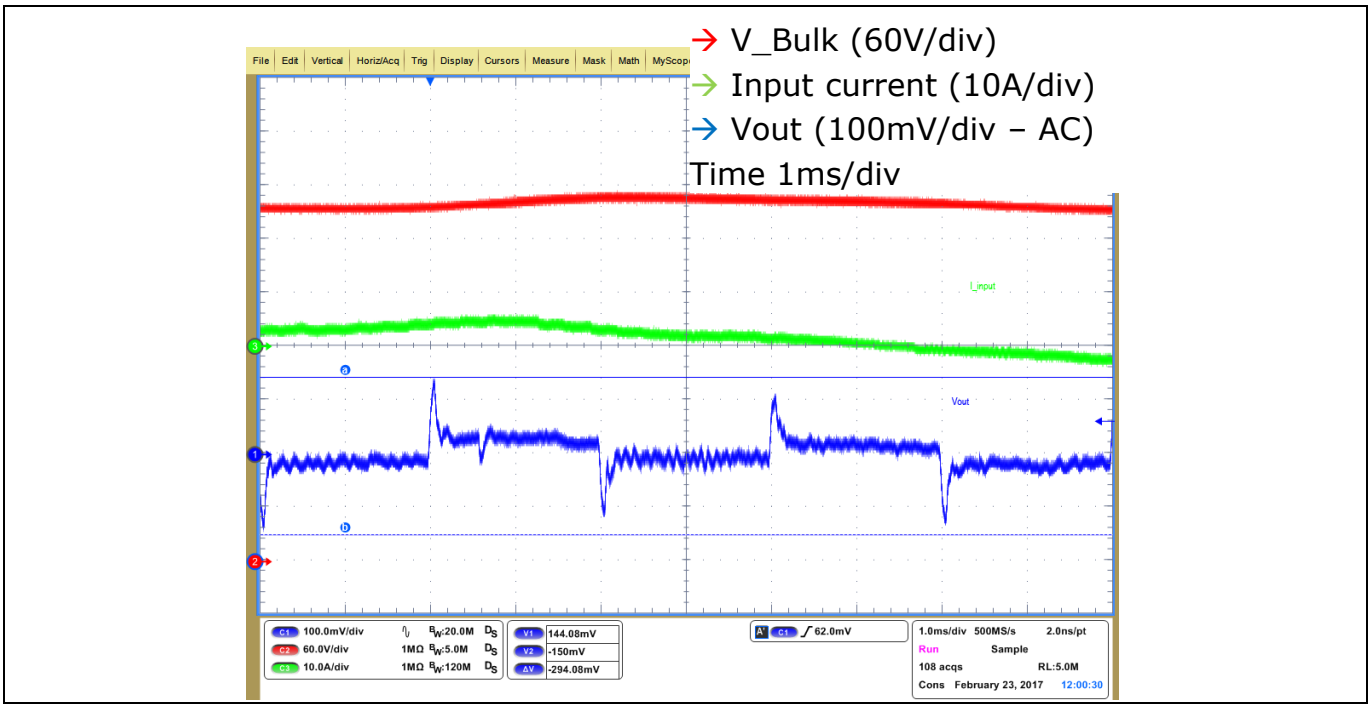

Figure 60 Load-step response 33–66 A at 0.5 A/µs

6.6 ABM operation

Under certain operating conditions, especially during light- or no-load operation, the bulk voltage can overshoot and the necessary LLC gain to keep regulation cannot be reached due to maximum frequency limitation. In this situation, ABM operation of the LLC is triggered if the output voltage is over 150 mV while operating at maximum frequency (300 kHz)

Figure 61 shows a load-dump from half- to no-load in which the ABM operation is triggered. The reduction of the bulk voltage leads to frequency reduction in the LLC converter, and therefore ABM operation is skipped.

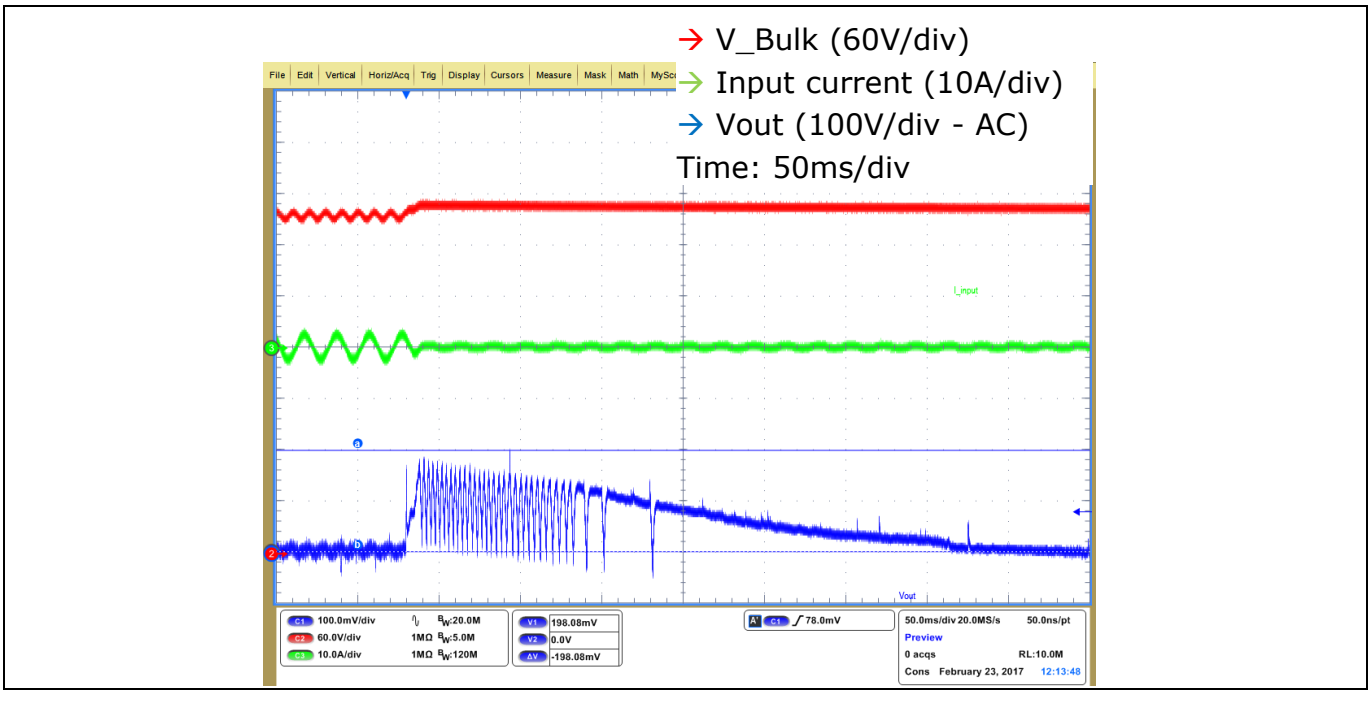

Figure 61 ABM operation during a half-load to no-load dump

6.7 Over Current Protection (OCP)

As shown in Figure 38, three different current levels with certain time allowances are programmed as OCP depending on the output CS. Figure 62 shows the system behavior when a load of 72 A is applied for more than 30 s, when the PSU was operating at half-load. In that case, the LLC stage is turned off, but not the PFC converter. A BVM can be noted due to the no-load operation of the boost converter. A similar situation is shown in Figure 63, where a 78 A load is applied for longer than 10 s. A third level of protection is set to 83 A. If this load is applied, the LLC converter turns off immediately, as shown in Figure 64.

For any of the three defined levels, the bulk voltage must decrease to under 330 V in order to clean the fault and restart the PSU with soft-start sequence for both the PFC and the LLC stages.

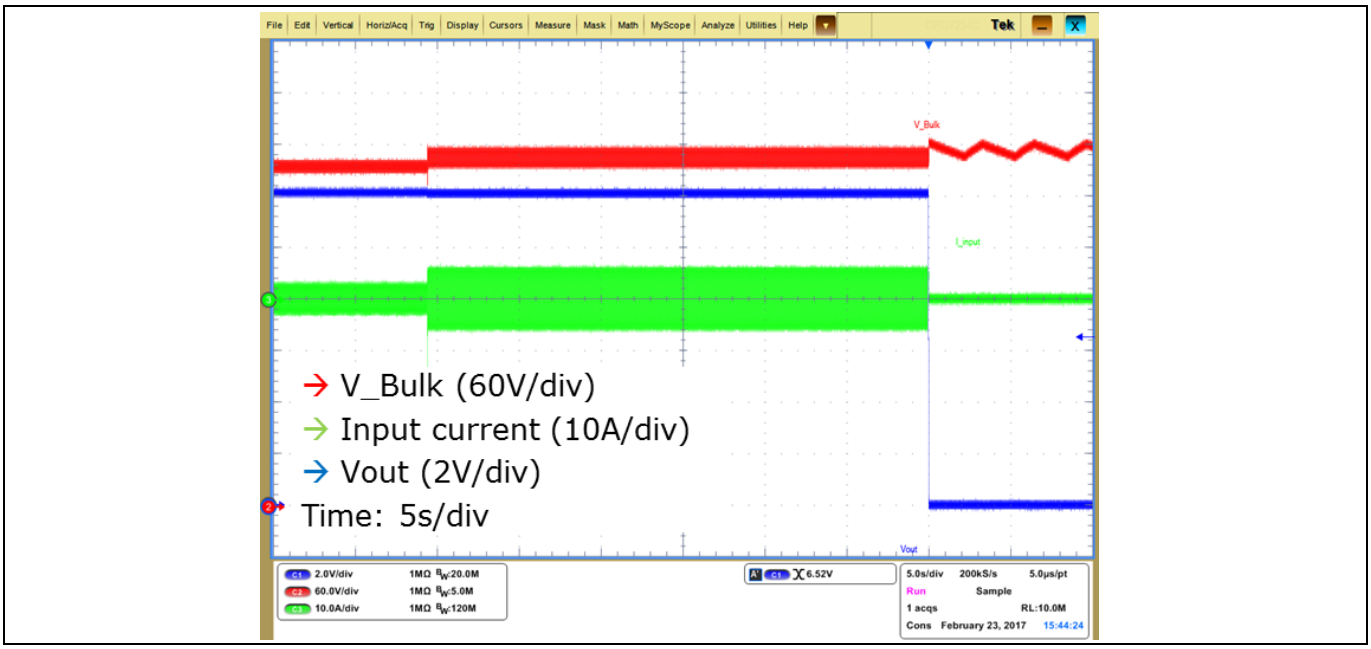

Figure 62 OCP triggered after 30 s with 72 A; step from half-load

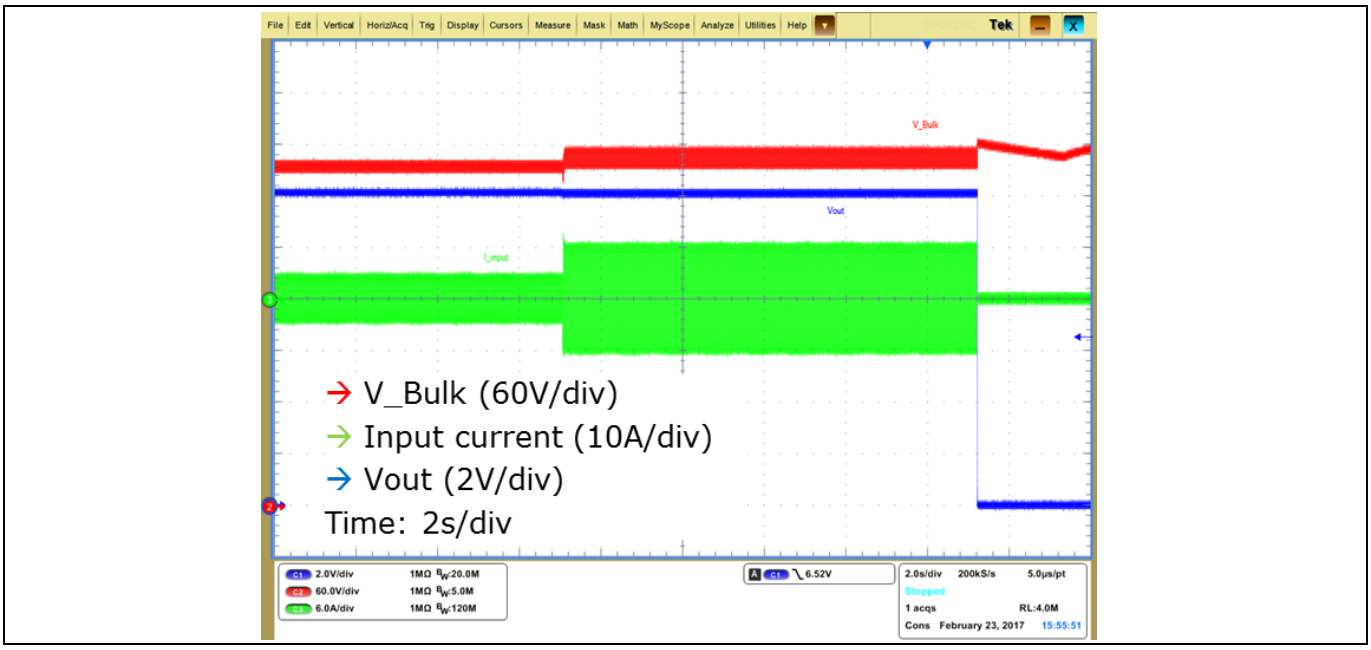

Figure 63 OCP triggered after 10 s with 78 A; step from half-load

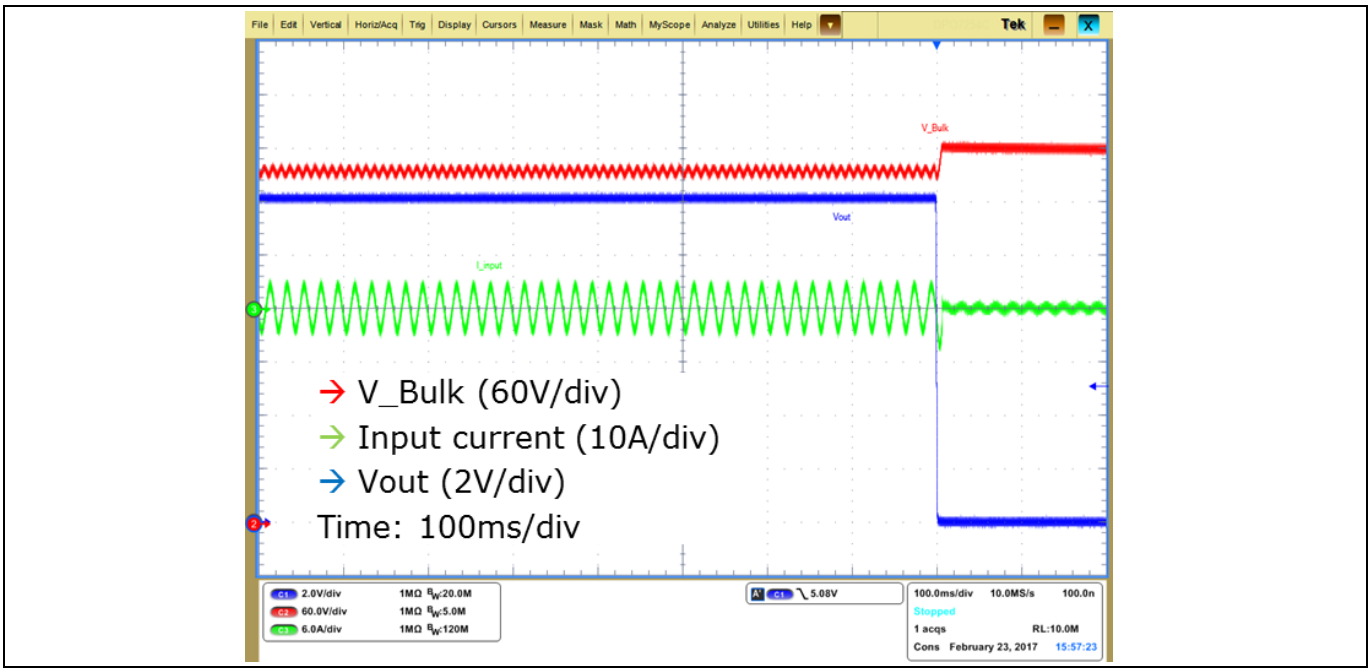

Figure 64 OCP triggered with 100 A (load short-circuit); step from half-load

6.7.1 Short-circuit

As explained in section 4.2.1 and 4.2.4, a resonant comparison protection is implemented. This allows fast detection of a short-circuit, given the fast reaction of the resonant current. Figure 65 shows the trigger for this protection, when a short-circuit is applied directly to the power supply output, and the consequent LLC operation stops. A controller reset is required to resume PSU operation.

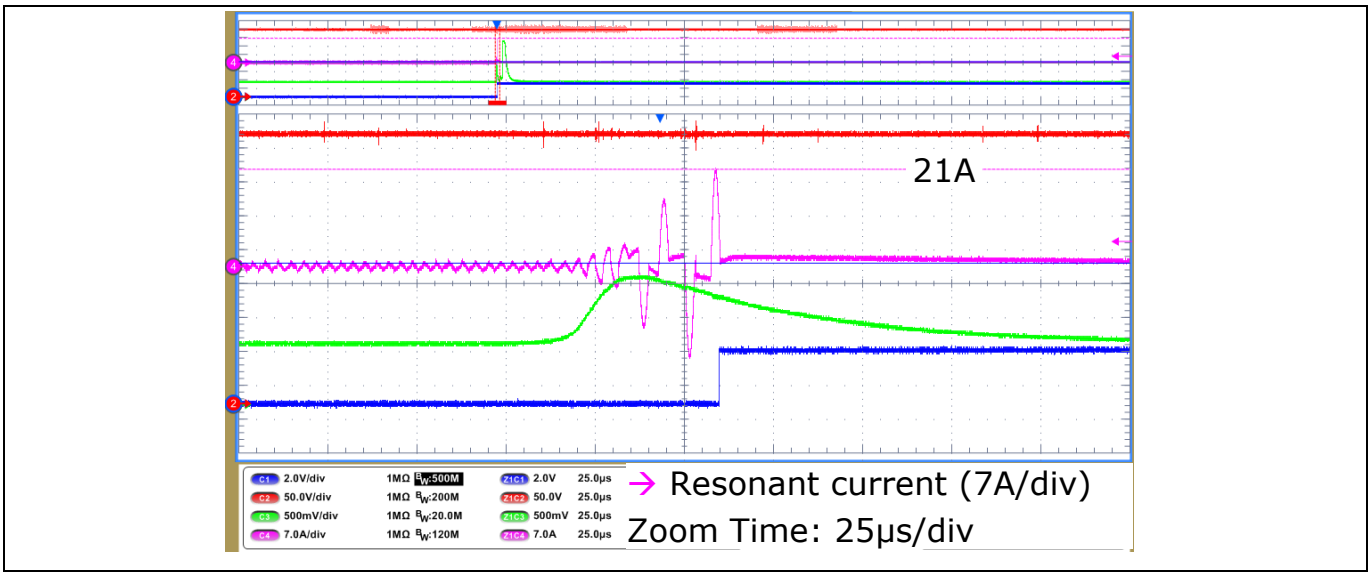

Figure 65 Resonant current comparison as short-circuit protection trigger

6.8 Conducted EMI (graphs)

The conducted EMI has been measured in the 800 W server power supply at full-load using resistive loads. The measurements are shown in Figure 66 and Figure 67 for 230 V and 90 V inputs, respectively. In the figures both peak (yellow) and average (blue) measurements are shown, together with the corresponding class B limit.

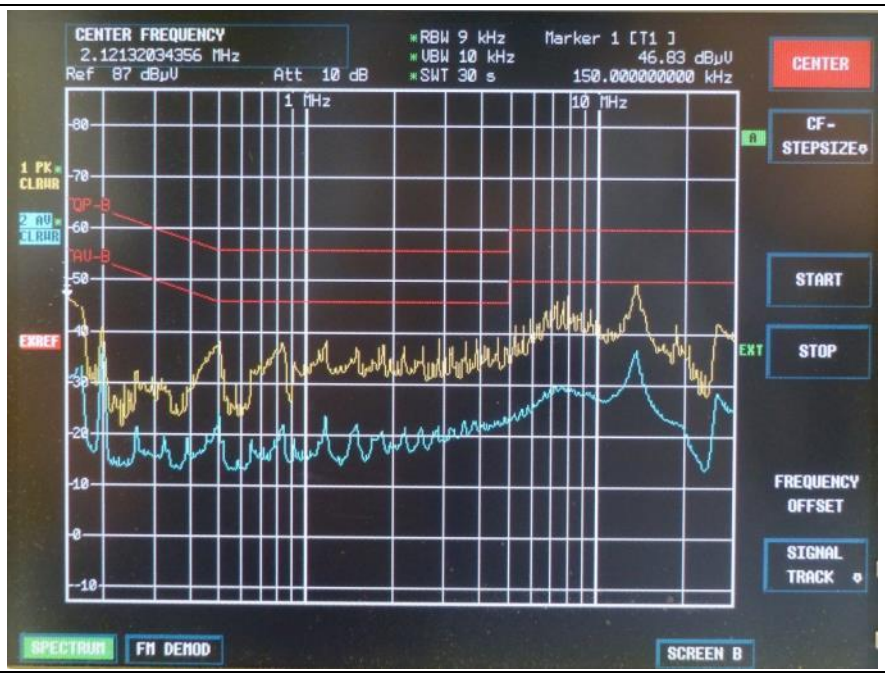

Figure 66 **Peak (yellow) and average (blue) conducted EMI measured with resistive load at full-load and 230 V input**

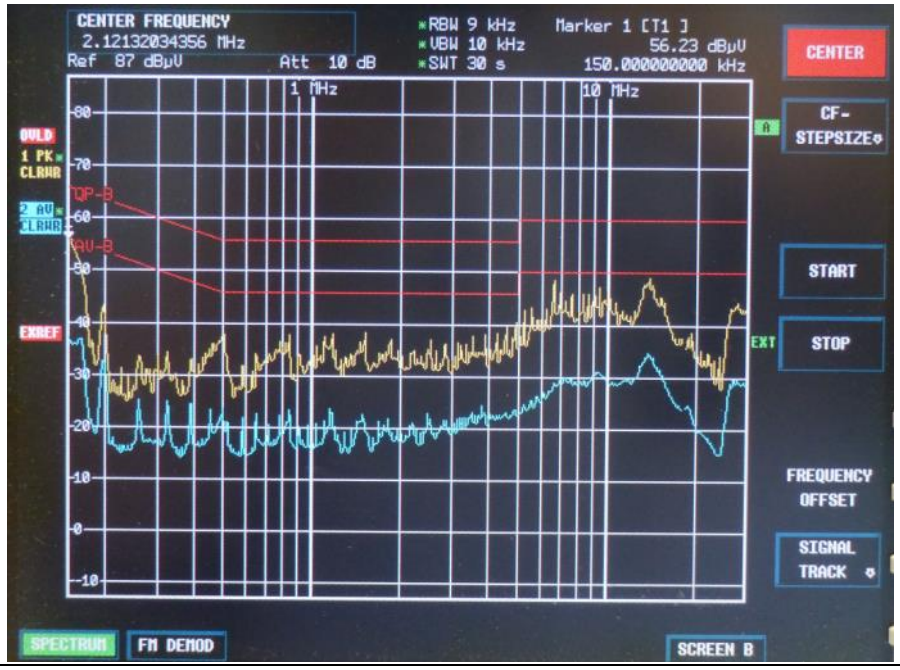

Figure 67 **Peak (yellow) and average (blue) conducted EMI measured with resistive load at full-load and 90 V input**

7 Schematics

7.1 Main board schematic

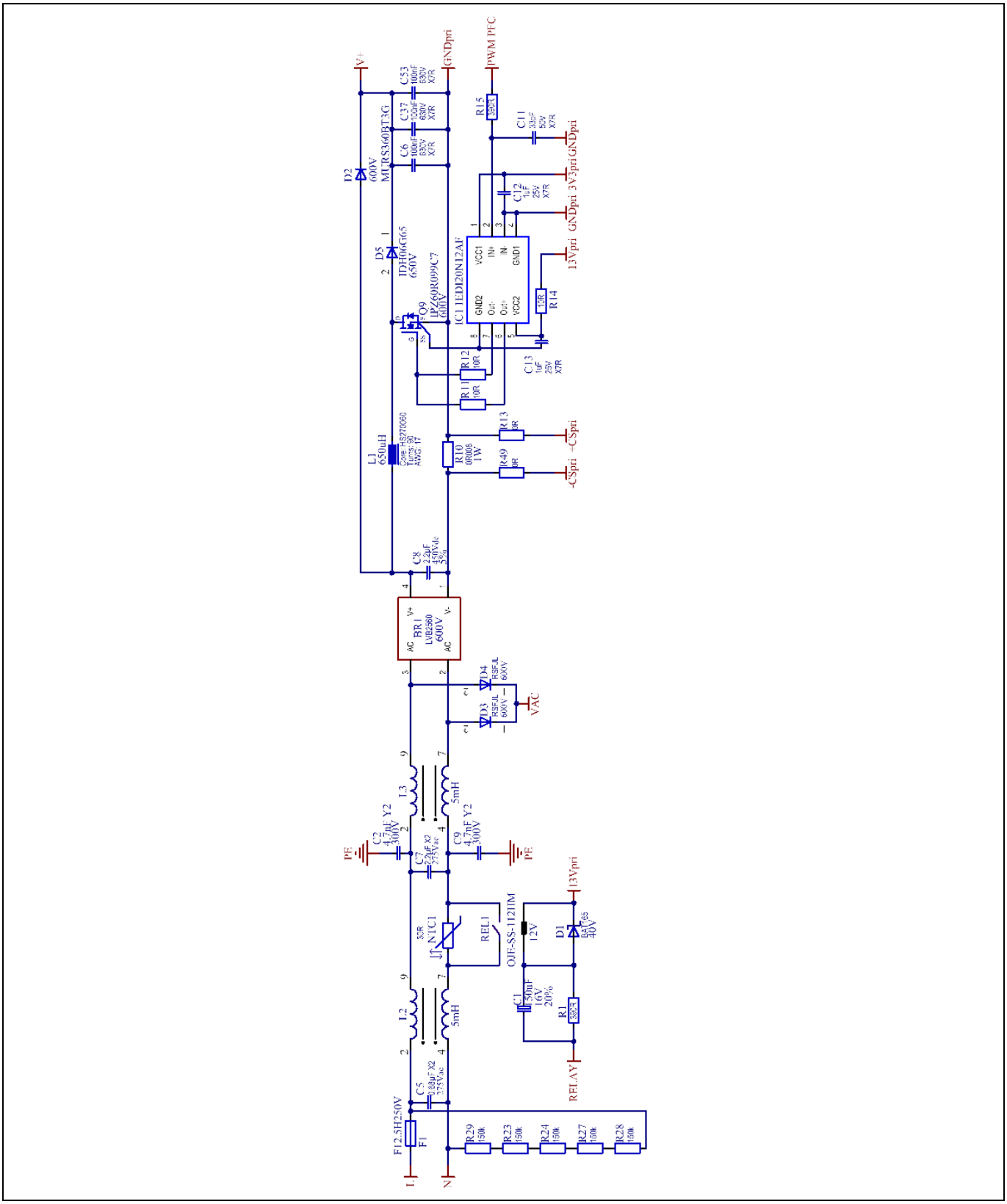

Figure 68 PFC stage schematic of the 800 W server power supply

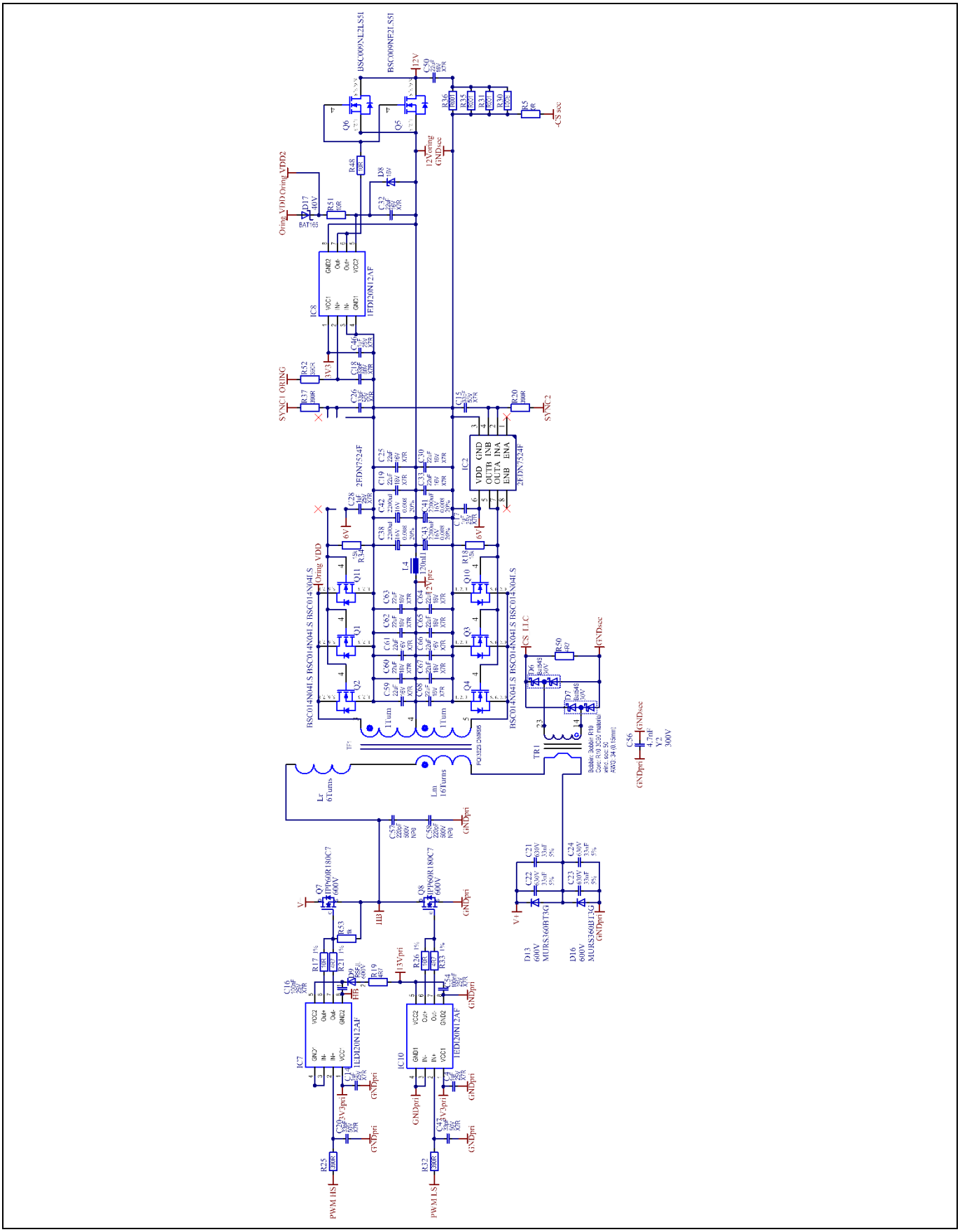

Figure 69 LLC stage schematic of the 800 W server power supply

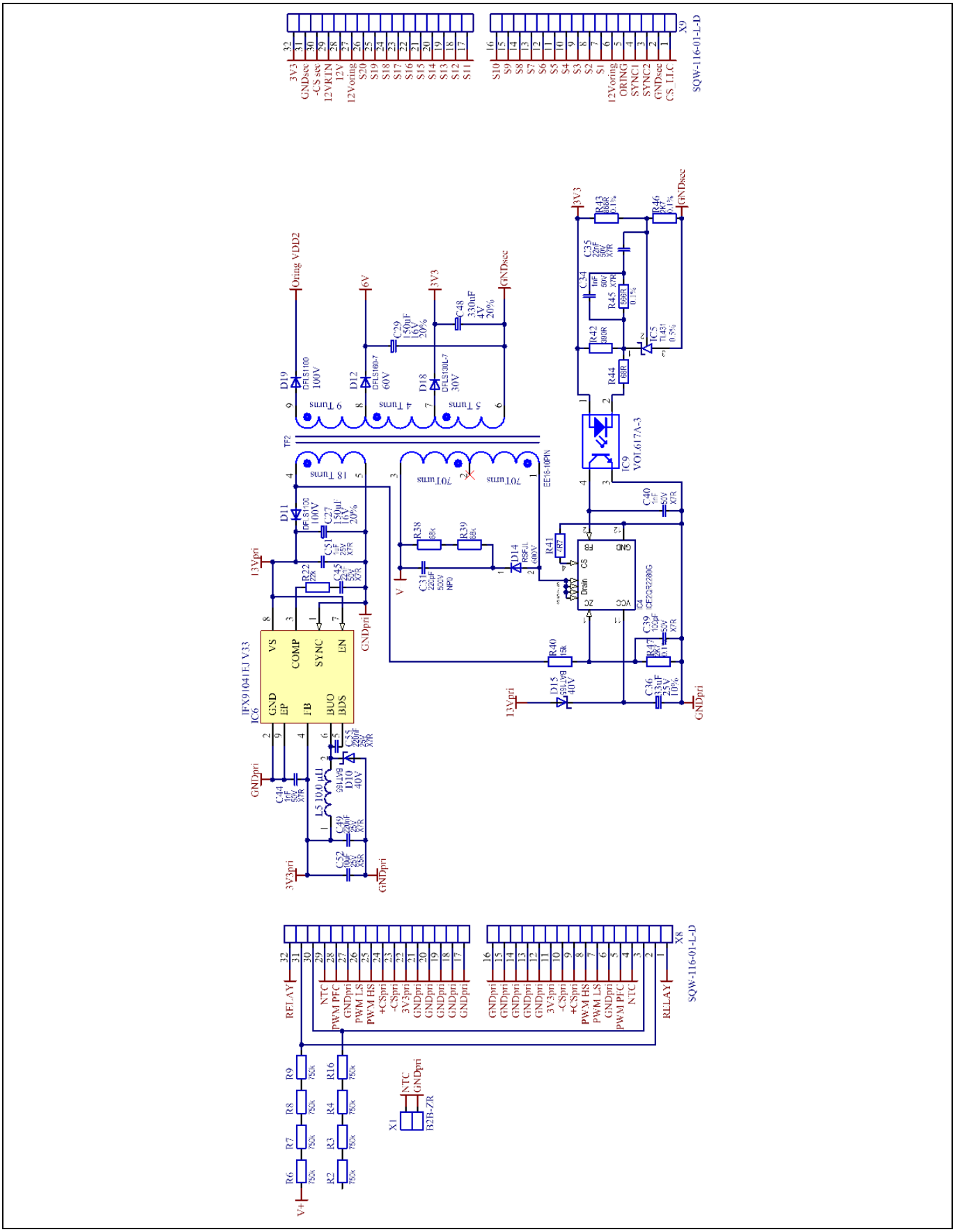

Figure 70 Auxiliary power supply schematic of the 800 W server power supply, including the connectors to the control board and the NTC temperature sensor

7.2 Control board schematic

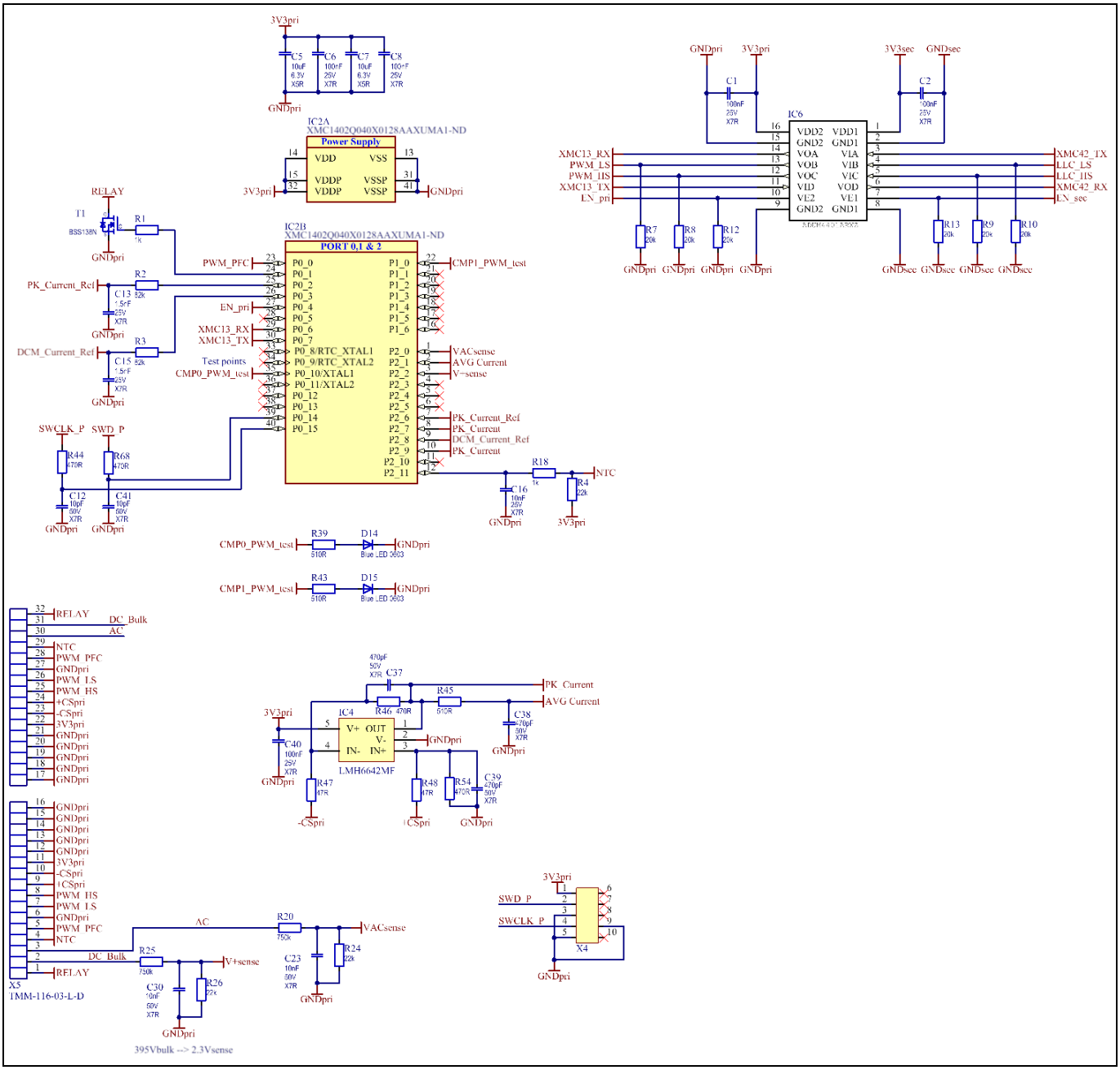

Figure 71 Primary-side controller (XMC1402) schematic, including the digital isolator for primary–secondary communication

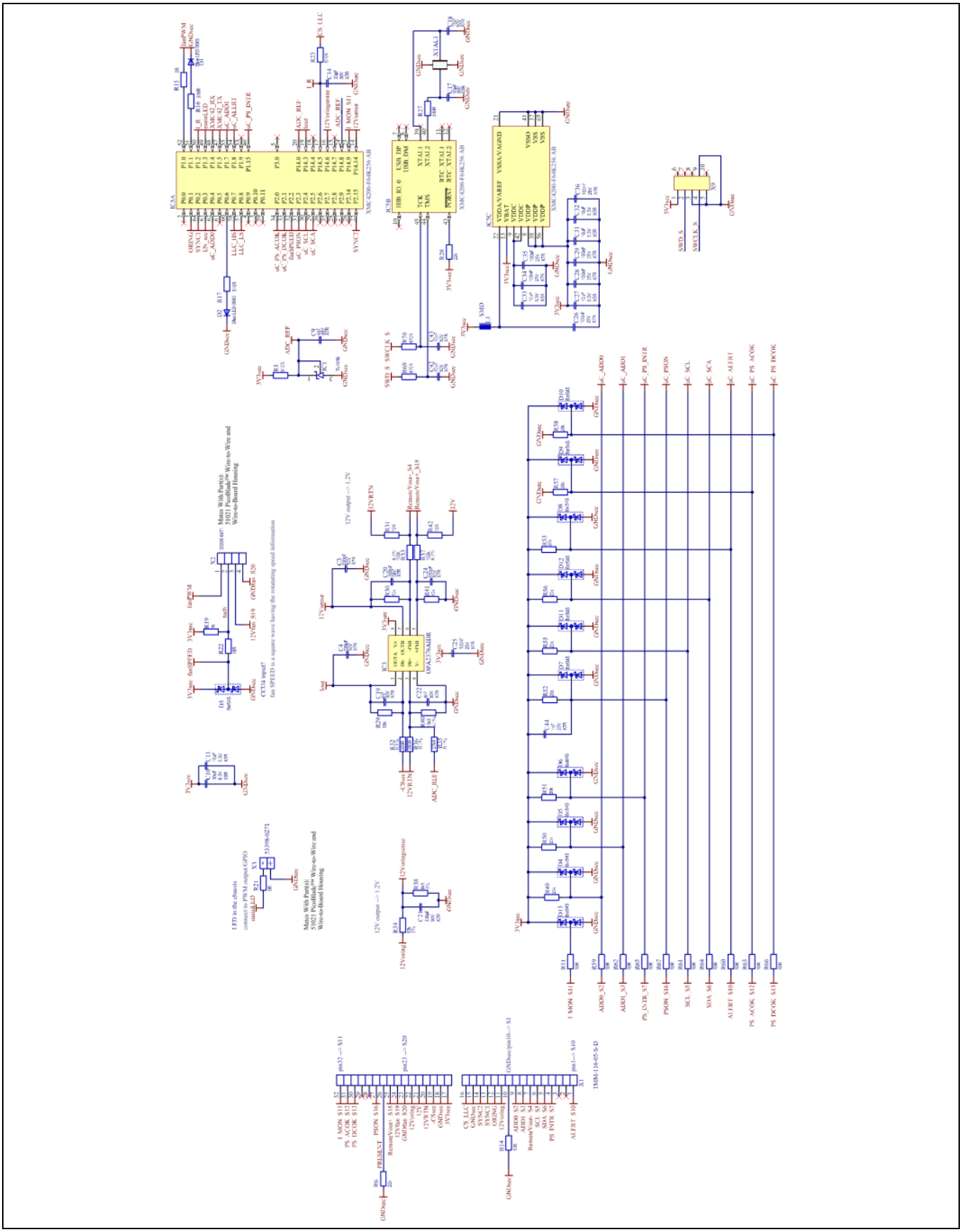

Figure 72 Secondary-side controller (XMC4200) schematic, including the signaling for the PSU output connector

8 Bill of Materials (BOM)

Table 10 Main board components

Designator	Comment	Value	Tolerance	Voltage	Description
C36	SMD	33 uF	10%	25 V	Capacitor polarized
C39	SMD	100 pF	X7R	50 V	Capacitor ceramic
C48	SMD	330 uF	20%	4 V	Capacitor polarized
C52	SMD	10 uF	X5R	25 V	Capacitor ceramic
D12	SMD	DFLS160-7		60 V	Standard diode
D18	SMD	DFLS130L-7		30 V	Standard diode
D8	SMD	BZT52C15		15 V	Zener diode
IC4	SMD	ICE2QR2280G			CoolSET® - Q1
IC5	SMD	TL431	0.5%		TL431- adjustable precision shunt regulator
IC6	SMD	IFX91041EJ V33	2(4)%		Integrated ciruit
IC9	SMD	VOL617A-3			Optocoupler
L4	SMD	120 nH			Output filter choke
L5	SMD	10.0 µH			Inductor
R1	SMD	390R	1%		Resistor
R10	SMD	0R008	1%		Resistor
R22	SMD	22k	1%		Resistor
R44	SMD	68R	1%		Resistor
C19, C25, C30, C32, C33, C50, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68	SMD	22 uF	X7R	16 V	Capacitor ceramic
C16, C54, C35	SMD	100 nF	X7R	25 V	Capacitor ceramic
C45	SMD	22 nF	X7R	50 V	Capacitor ceramic
C49, C55	SMD	220 nF	X7R	25 V	Capacitor ceramic
D11, D19	SMD	DFLS1100		100 V	Standard diode
D6, D7	SMD	Bat54S		30 V	
IC2, IC3	SMD	2EDN7524F			2EDN752x / 2EDN852x
Q5, Q6	SMD	BSC009NE2LS5I		25 V	N-Channel OptiMOS™ 5 Power-transistor, 25 V VDS, 100 A ID, -55 to 150 degC, PG-TDSON-8-1, Reel, Green
R14, R51	SMD	10R	1%		Resistor
R21, R33	SMD	4R7	1%		Resistor
R38, R39	SMD	68k	1%		Resistor
R43, R45	SMD	866R	0.1%		Resistor
R46, R47	SMD	2k7	0.1%		Resistor
C1, C27, C29	SMD	150 uF	20%	16 V	Capacitor polarized
C31, C57, C58	SMD	220 pF	NP0	500 V	Capacitor ceramic
C34, C40, C44	SMD	1 nF	X7R	50 V	Capacitor ceramic
C6, C37, C53	SMD	100 nF	X7R	630 V	Capacitor ceramic

Bill of Materials (BOM)

Designator	Comment	Value	Tolerance	Voltage	Description
D2, D13, D16	SMD	MURS360BT3G		600 V	Standard diode
R18, R34, R40	SMD	15k	1%		Resistor
R19, R41, R50	SMD	4R7	1%		Resistor
R5, R13, R49	SMD	0R	1%		Resistor
D1, D10, D15, D17	SMD	BAT165		40 V	Schottky diode
D3, D4, D9, D14	SMD	RSFJL		600 V	Diode
IC1, IC7, IC8, IC10	SMD	1EDI20N12AF			Single-channel MOSFET gate driver IC
R30, R31, R35, R36	SMD	R001	1%		Resistor
R11, R12, R17, R26, R48	SMD	10R	1%		Resistor
R23, R24, R27, R28, R29	SMD	150k	1%		Resistor
C11, C15, C18, C20, C26, C47	SMD	33 pF	X7R	50 V	Capacitor – ceramic
Q1, Q2, Q3, Q4, Q10, Q11	SMD	BSC010N04LSI		40 V	N-channel OptiMOS™ 5 power-transistor, 40 V VDS, 100 A ID, -55–150°C, PG-TDSON-8-1, Reel, Green
R15, R20, R25, R32, R37, R42, R52	SMD	390R	1%		Resistor
C4, C12, C13, C14, C17, C28, C46, C51	SMD	1 uF	X7R	25 V	Capacitor – ceramic
R2, R3, R4, R6, R7, R8, R9, R16	SMD	750k	1%		Resistor
BR1	THT	LVB2560		600 V	
C5	THT	0.22 µF X2	20%	275 V AC	Capacitor – foil
C7	THT	2.2 µF X2	20%	275 V AC	Capacitor – foil
C8	THT	2.2 µF	5%	450 V DC	Capacitor – foil
D5	THT	IDH06G65		650 V	Diode – SiC
F1	THT	F12.5H250 V			Sicherung
L1	THT	650 uH			PFC choke
NTC1	THT	30R	±20%		NTC resistor
Q9	THT	IPZ60R099C7		600 V	n-MOSFET with source sense
REL1	THT	OJE-SS-112HM		12 V	Relais Schließer
TF1	THT	PQI3523 DMR95			Main transformer
TF2	THT	EE16-10PIN			Bias transformer
TR1	THT				CS transformer
X1	THT	B2B-ZR			Pin header 2-pole
C2, C9	THT	1.5 nF	Y2	300 V	Capacitor – ceramic
L2, L3	THT	5 mH			CM power line choke

Designator	Comment	Value	Tolerance	Voltage	Description
Q7, Q8	THT	IPP60R180C7		600 V	n-MOSFET
X8, X9	THT	SQW-116-01-L-D			Pin header 2 × 16 contacts
C3, C10, C56	THT	2.2 nF	Y2	300 V	Capacitor – ceramic
C21, C22, C23, C24	THT	27 nF	5%	630 V	Capacitor – foil
C38, C41, C42, C43	THT	2200 uF	20%	16 V	Capacitor – electrolyte
C69	THT	4700 uF	20%	450 V	Capacitor – electrolyte

Table 11 Control board components

Designator	Comment	Value	Tolerance	Voltage	Description
C1, C2, C6, C8, C25, C26, C28, C29, C34, C35, C36, C40	SMD	100 nF	X7R	25 V	Capacitor – ceramic
C3, C4, C20, C21, C24	SMD	330 pF	X7R	50 V	Capacitor – ceramic
C5, C7, C10, C11, C27, C31, C32, C33	SMD	10 uF	X5R	6.3 V	Capacitor – ceramic
C9, C19, C22	SMD	4n7	X7R	50 V	Capacitor – ceramic
C12, C41, C42, C43	SMD	10 pF	X7R	50 V	Capacitor – ceramic
C13, C15	SMD	1.5 nF	X7R	25 V	Capacitor – ceramic
C14	SMD	33 pF	X7R	50 V	Capacitor – ceramic
C16	SMD	10 nF	X7R	25 V	Capacitor – ceramic
C17, C18	SMD	15 pF	X7R	50 V	Capacitor – ceramic
C23, C30	SMD	10 nF	X7R	50 V	Capacitor – ceramic
C37, C38, C39	SMD	470 pF	X7R	50 V	Capacitor – ceramic
D1, D2, D14, D15	SMD	Blue LED 0603			Diode – LED
D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13	SMD	Bat54S			Diode
IC1	SMD	TL431B			IC
IC2	SMD	XMC1402Q040X0128A AXUMA1-ND			IC
IC3	SMD	OPA2376AIDR			IC
IC4	SMD	LMH6642MF			IC
IC5	SMD	XMC4200-F64K256 AB			IC
IC6	SMD	ADUM4401ARWZ			IC
L1	SMD	Ferrite bead 60 Ω @100 MHz			Inductor
R1, R18, R19	SMD	1k	1%		Resistor
R2, R3, R34	SMD	82k	1%		Resistor
R4, R6, R24, R28	SMD	22k	1%		Resistor
R26	SMD	22k	0.1%		Resistor
R5, R16, R17, R23, R27, R39, R43, R45	SMD	510R	1%		Resistor
R7, R8, R9, R10, R12, R13, R49, R50, R51, R52, R53, R55, R56,	SMD	20k	1%		Resistor

Bill of Materials (BOM)

Designator	Comment	Value	Tolerance	Voltage	Description
R57, R58					
R11, R14, R22, R31, R42, R59, R60, R61, R62, R63, R64, R65, R66, R67	SMD	10R	1%		Resistor
R15, R21	SMD	0R	1%		Resistor
R20, R25	SMD	750k	1%		Resistor
R29, R30, R41	SMD	10k	0.1%		Resistor
R32, R36	SMD	200R	0.1%		Resistor
R33, R37	SMD	100k	0.1%		Resistor
R35	SMD	27k4	0.1%		Resistor
R38	SMD	9k1	1%		Resistor
R40	SMD	15k8	0.1%		Resistor
R44, R46, R54, R68, R69, R70	SMD	470R	1%		Resistor
R47, R48	SMD	47R	1%		Resistor
T1	SMD	BSS138N			MOSFET
X1	SMD	TMM-116-05-S-D			Pin header 2 × 16 contacts
X2	SMD	53398-0471			Pin header 4 contacts
X3	SMD	53398-0271			Pin header
X4, X9	SMD				Pin header 2 × 5 contacts
X5	SMD	TMM-116-03-L-D			Pin header 2 × 16 contacts
XTAL1	SMD	12 MHz			Crystal oscillator

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Revision history

Major changes since the last revision

Page or reference	Description of change

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