3300 W 54 V bi-directional phase-shift full-bridge with 600 V CoolMOS™ CFD7 and XMC™

EVAL_3K3W_BIDI_PSFB

About this document

Authors:

Matteo-Alessandro Kutschak, Escudero Rodriguez Manuel

Scope and purpose

This document introduces a complete Infineon Technologies AG system solution for a 3300 W bi-directional DC-DC converter that achieves 98 percent efficiency in buck mode and 97 percent in boost mode. The EVAL_3K3W_BIDI_PSFB board is a DC-DC stage with telecom-level output realized by a Phase-Shift Full-Bridge (PSFB) topology block with bi-directional capability.

This document shows the board using CoolMOS™ CFD7 and OptiMOS™ 5 in a full SMD solution with an innovative cooling concept.

The Infineon components used in the 3300 W bi-directional PSFB are:

- 600 V CoolMOS™ CFD7 superjunction (SJ) MOSFET
- 150 V OptiMOS™ 5 Synchronous Rectifier (SR) MOSFET
- 2EDS8265H safety isolated and 2EDF7275F functional isolated gate drivers (EiceDRIVER™)
- XMC4200-F64k256AB microcontroller
- ICE5QSAG CoolSET™ Quasi Resonant (QR) flyback controller
- 800 V CoolMOS™ P7 Superjunction (SJ) MOSFET
- CoolSiC™ Schottky diode 650 V G6 (IDH08G65C6)
- Medium-power Schottky diode BAT165
- IFX91041EJV33 DC-DC step-down voltage regulator

Figure 1 **3300 W bi-directional PSFB**

Intended audience

This document is intended for SMPS designers and engineers who want to improve their HV applications to achieve increased power density and the highest energy efficiency.

Table of contents

About this document **1**
Table of contents **3**
1 Background and system description **4**
1.1 System description 5
1.2 Board description 6
1.3 CoolMOS™ CFD7 7
1.3.1 CoolMOS™ CFD7 $R_{DS(on)}$ comparison 8
1.3.2 CoolMOS™ CFD2 comparison 10
1.4 Transformer 12
1.5 Cooling solution 14
1.6 EiceDRIVER™ 2EDSx reinforced, 2EDFx functional isolated gate driver 15
1.7 Validation set-up 18
1.7.1 Buck mode 18
1.7.2 Boost mode 18
2 Buck mode results **20**
2.1 Specification and test results 20
2.2 Performance and steady-state waveforms 20
2.2.1 HV full-bridge 20
2.2.2 Synchronous rectifiers 22
2.2.3 Dynamic response 22
2.2.4 Start-up 23
2.2.5 Burst mode 24
2.2.6 Constant power limitation 24
2.3 Thermal map 25
3 Boost **27**
3.1 Operation 27
3.2 Performance and steady-state waveforms 27
3.2.1 HV full-bridge 27
3.2.2 LV bridge 28
3.2.3 Start-up 29
3.2.4 Burst mode 30
3.3 Thermal map 31
4 User interface **33**
5 Summary **35**
6 Schematics **36**
7 Bill of Materials (BOM) **39**
8 References **42**
Revision history 43

1 Background and system description

The trend in SMPS in recent years has been toward increased power density with optimized cost. Achieving this higher power density, high efficiency is a key parameter, since heat dissipation must be minimized.

Toward this goal, fully resonant topologies like LLC are often considered to be the best approach in this power range and voltage class [5]. However, the 3300 W bi-directional PSFB is an example of how the improvement in semiconductor technology and control algorithms allows a simple and well-known topology block like PSFB to reach the high efficiency levels traditionally considered out of reach for this topology.

Furthermore, for the construction of a bi-directional DC-DC stage an LLC or a dual active bridge topology would be the most common approach [4]. We demonstrate here, thanks to the flexibility of digital control, that the traditional PSFB topology block can be used as a bi-directional DC-DC converter without changes on what would be otherwise a standard PSFB design.

The efficiency shown in Figure 2 can be achieved by using the best-in-class 600 V CoolMOS™ CFD7 in a Surface Mount Device (SMD) package together with 150 V OptiMOS™ 5 synchronous rectifiers. The outstanding performance of these semiconductor technologies, the innovative cooling concept for a full SMD solution and the stacked magnetic construction achieves a power density in the range of 4.34 W/cm^3 (71.19 W/in^3). Due to production tolerances, efficiency variations in the range of 0.1 percent could be seen in the result shown.

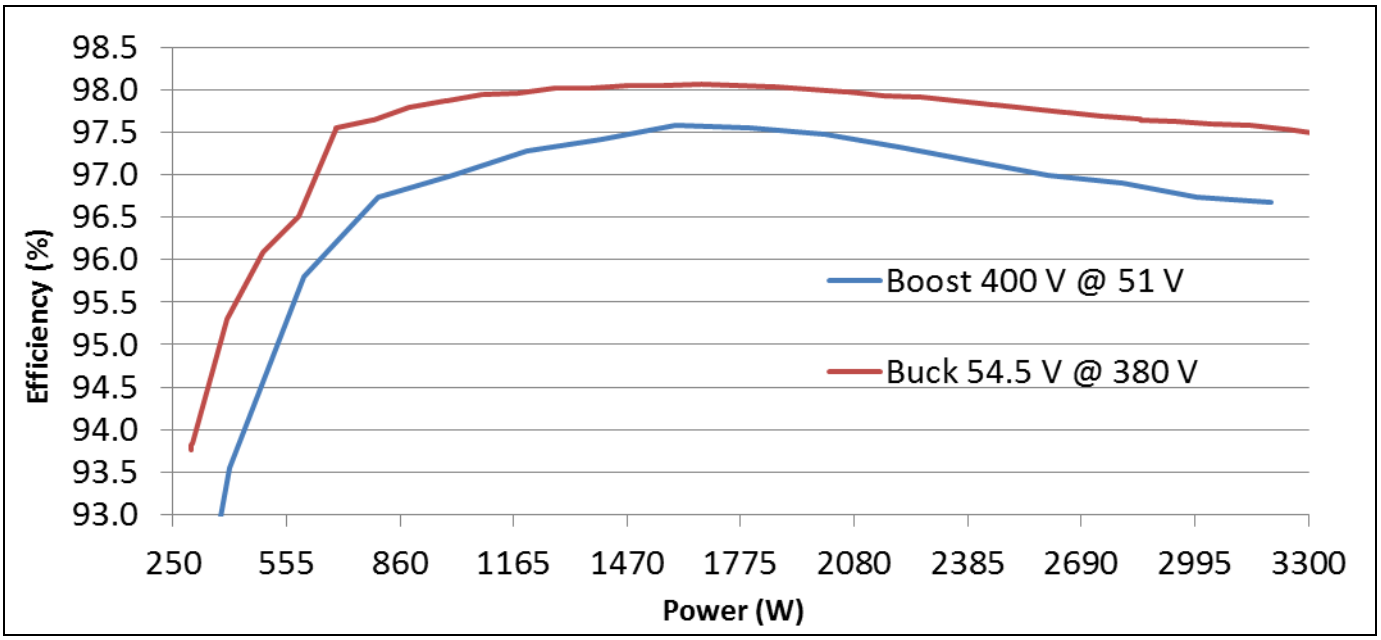

Figure 2 Measured efficiency of bi-directional 3300 W PSFB (fan consumption included)

The 3300 W bi-directional PSFB is a DC-DC converter developed with Infineon power semiconductors as well as Infineon drivers and controllers. The Infineon devices used in the implementation of the 3300 W bi-directional PSFB are:

- 75 mΩ 600 V CoolMOS™ CFD7 (IPL60R075CFD7) in the HV bridge
- 9.3 mΩ 150 V OptiMOS™ 5 in Super SO-8 package (BSC093N15NS) in the LV bridge
- 2EDS8265H safety isolated and 2EDF7275F functional isolated gate drivers (EiceDRIVER™)
- ICE5QSAG QR flyback controller with external 800 V CoolMOS™ P7 4.5Ω (IPU80R4K5P7) for the auxiliary supply [2]
- XMC4200 microcontroller for control implementation (XMC4200-F64k256AB)

- CoolSiC™ Schottky diode 650V G6 (IDH08G65C6)
- Medium-power Schottky diode BAT165
- IFX91041EJV33 DC/DC step-down voltage regulator

This document will describe the system and board of the 3300 W bi-directional PSFB, as well as the specifications and main test results. For further information on Infineon semiconductors see the Infineon website, as well as the Infineon evaluation board search, and the different websites for the different implemented components:

- CoolMOS™ power MOSFETs
- OptiMOS™ power MOSFETs
- Gate driver ICs
- QR CoolSET™
- XMC™ microcontrollers
- CoolSiC™ Schottky diode

1.1 System description

The EVAL_3K3W_BIDI_PSFB design consists of a PSFB with SR in full-bridge configuration (Figure 3).

The control is implemented in an XMC4200 Infineon microcontroller, which includes voltage regulation functionality with peak current mode control, burst mode operation, output Over-Current Protection (OCP), Over-Voltage Protection (OVP), soft-start, SR control, adaptive timings (bridge and synchronous rectifiers) and serial communication interface. Further detail about the digital control implementation and further functionalities of PSFB in the XMC™ 4000 family can be found in [1], [2].

The converter's nominal output is telecom-level voltage class (54.5 V) or that of a 48 V battery charger working range (60 V to 40 V). The stage is operated at a nominal input voltage of 400 V, whereas it can regulate down to 360 V at full load (54.5 V nominal output voltage), providing room for hold-up time whenever the design is part of a full AC-DC converter.

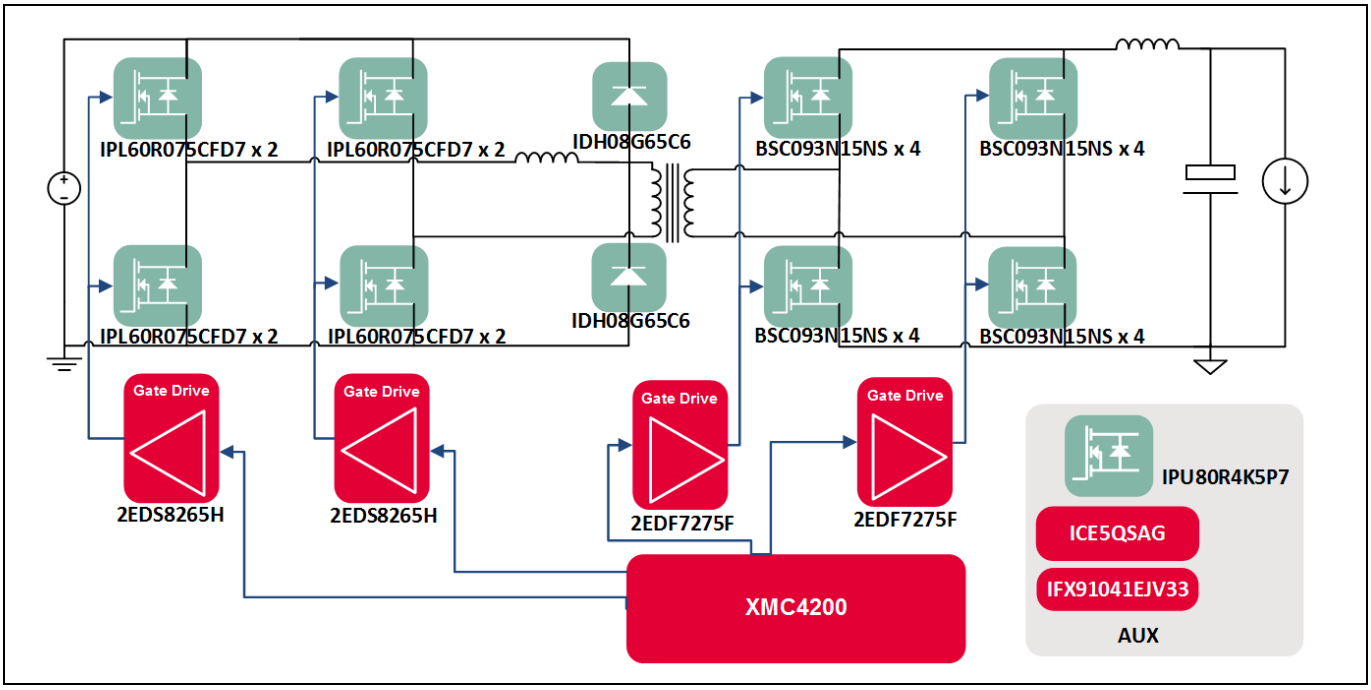

Figure 3 **3300 W bi-directional PSFB (EVAL_3K3W_BIDI_PSFB) – simplified diagram showing the Infineon semiconductors used**

The switching frequency of the converter is 100 kHz. The design was optimized for frequencies in the range of 110 kHz to 90 kHz, as can be seen in the efficiency versus frequency estimation curves for the 40 percent, 50 percent and 60 percent load points in Figure 4.

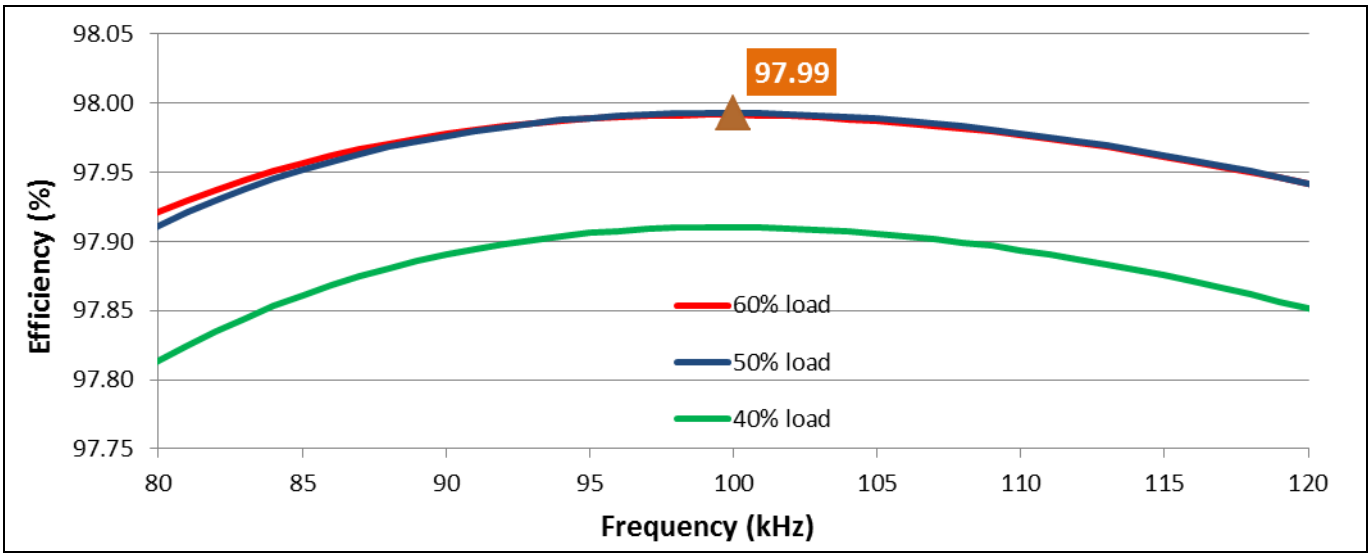

Figure 4 **Estimated efficiency of 3300 W bi-directional PSFB in buck mode at different switching frequencies (fan consumption not considered) for the load points of interest**

1.2 Board description

Figure 5 shows the placement of the different components on the 3300 W bi-directional PSFB. The outer dimensions of the board, enclosed in the case, are 208 mm x 83 mm x 44 mm, which results a power density in the range of 4.34 W/cm³ (71.19 W/in³).

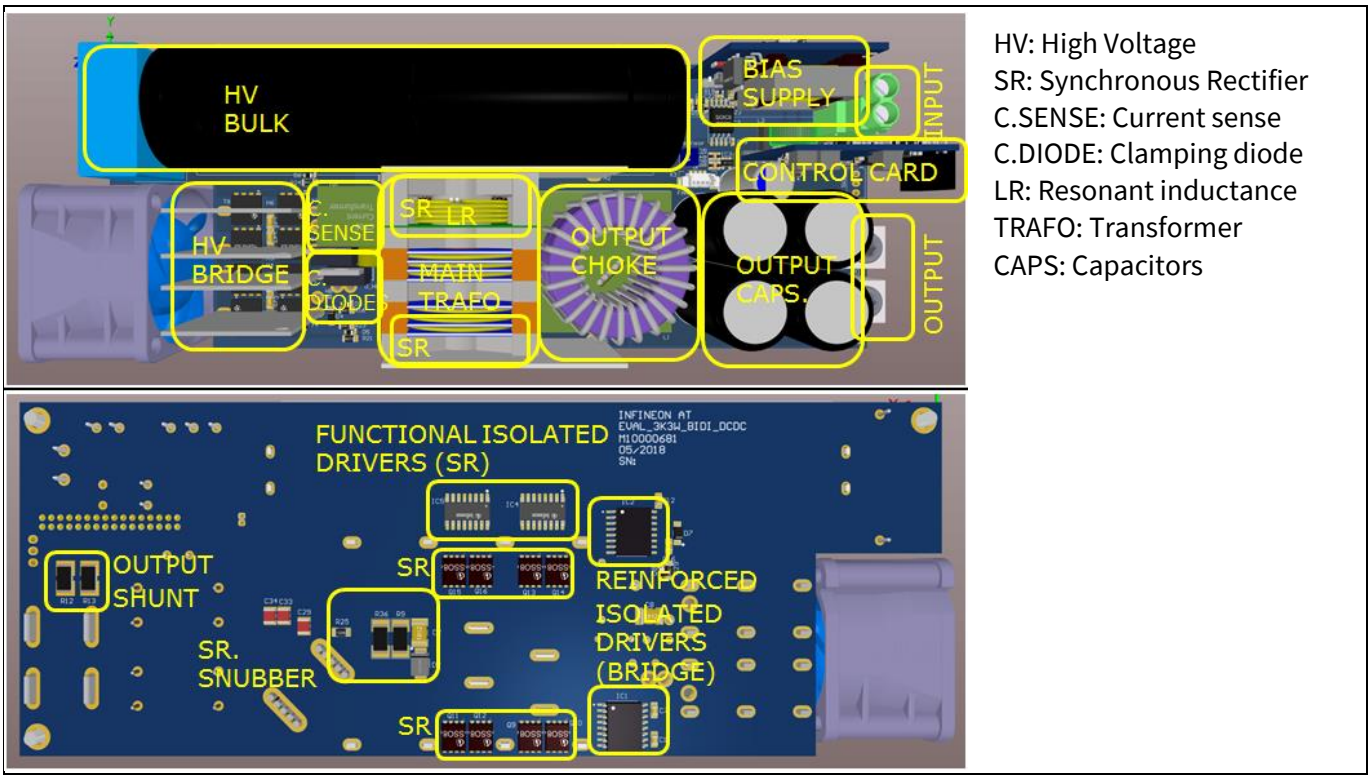

Figure 5 **Placement of the different sections in the 3300 W bi-directional PSFB with Infineon CoolMOS™ CFD7 and OptiMOS™ 5**

The estimated overall distribution of losses of the converter along the load proves the transformer and other magnetics as the main sources of loss (Figure 6). The semiconductors, both 600 V CoolMOS™ CFD7 and 150 V OptiMOS™ 5, are best-in-class performance parts and exhibit a good balance of switching to conduction loss.

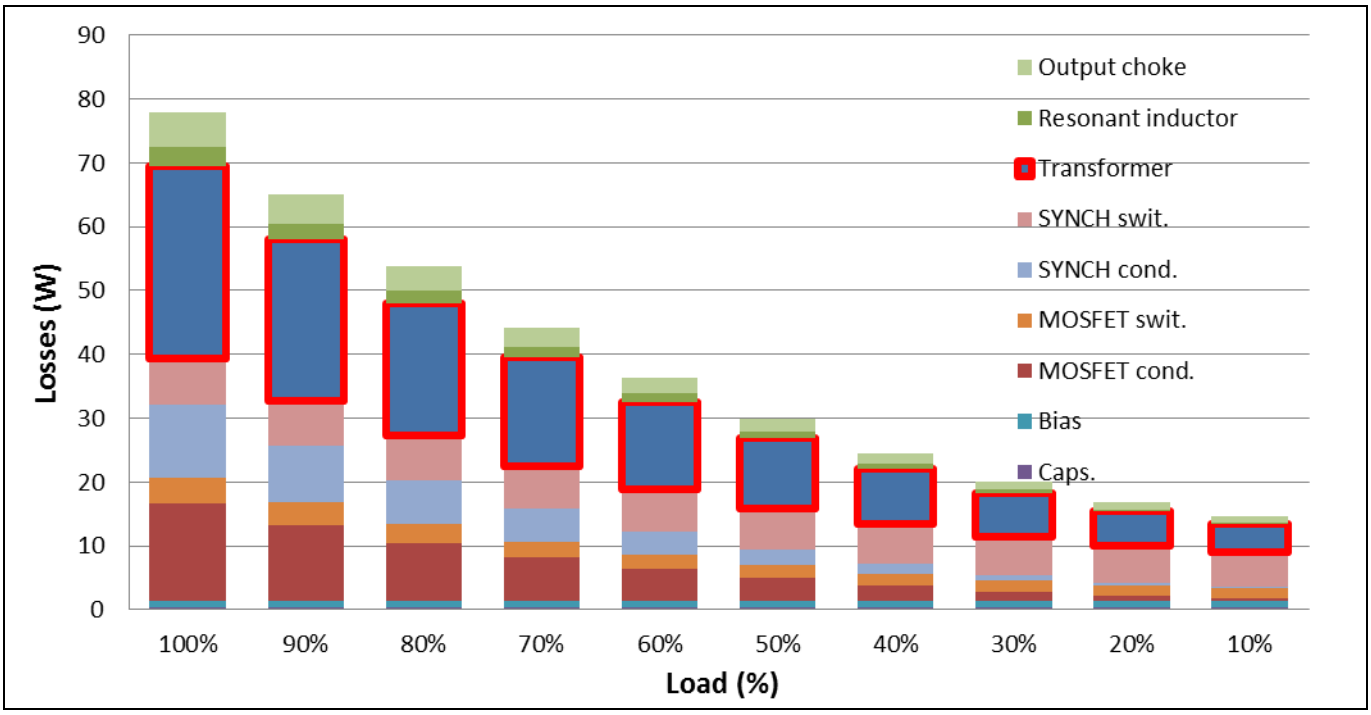

Figure 6 **Overall losses breakdown of 3300 W bi-directional PSFB in buck mode along load**

As highlighted by Figure 6, the great performance of the semiconductors makes the magnetic loss contribution the major percentage in terms of losses in most of the working conditions of the converter.

1.3 CoolMOS™ CFD7

IPL60R075CFD7 stands for the 75 mΩ 600 V CoolMOS™ CFD7 in ThinPAK package, the latest and best-performing fast body diode device from Infineon.

IPL60R075CFD7 brings a low loss contribution along all load ranges and exhibits a good balance of conduction to switching losses at the 50 percent load point, becoming the right device and $R_{DS(on)}$ class when optimizing for high peak efficiency at that point (Figure 7).

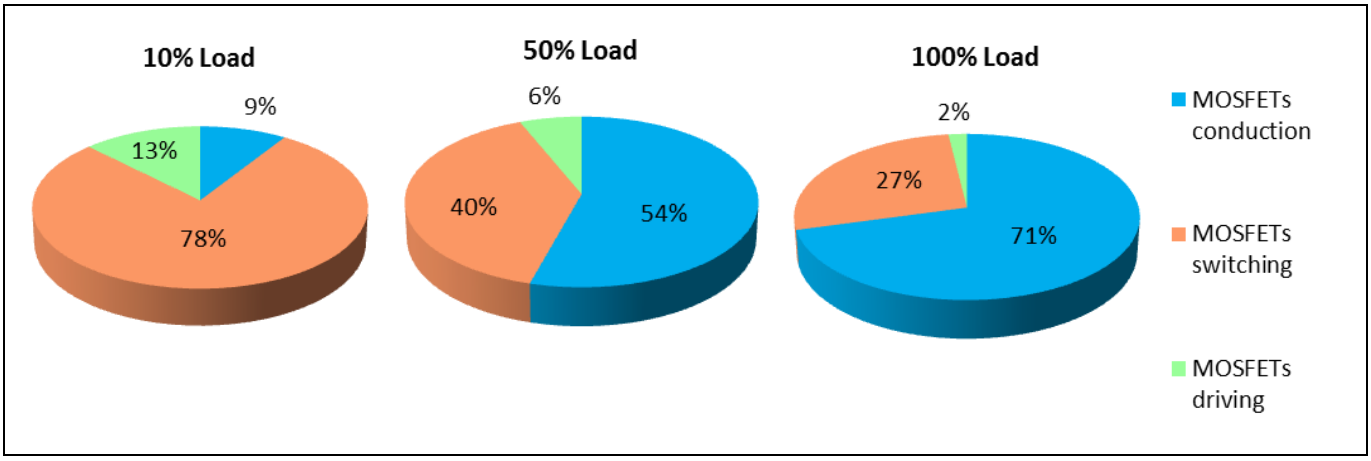

Figure 7 **IPL60R075CFD7 loss distribution (percentage of MOSFET contribution) along load in the 3300 W bi-directional PSFB in buck mode**

For a better distribution of power losses and improved cooling performance of the SMD devices, every position of the HV bridge is composed of two IPL60R075CFD7s in parallel (Figure 8). This configuration brings the benefit of half the nominal $R_{DS(on)}$ plus the additional benefit of the devices running at a lower temperature (with lower $R_{DS(on)}$ increase due to temperature).

The driving circuitry includes a single external resistor for two devices, because IPL60R075CFD7 includes an embedded Rg (5.9 Ω) – big enough for safe parallel operation in this application.

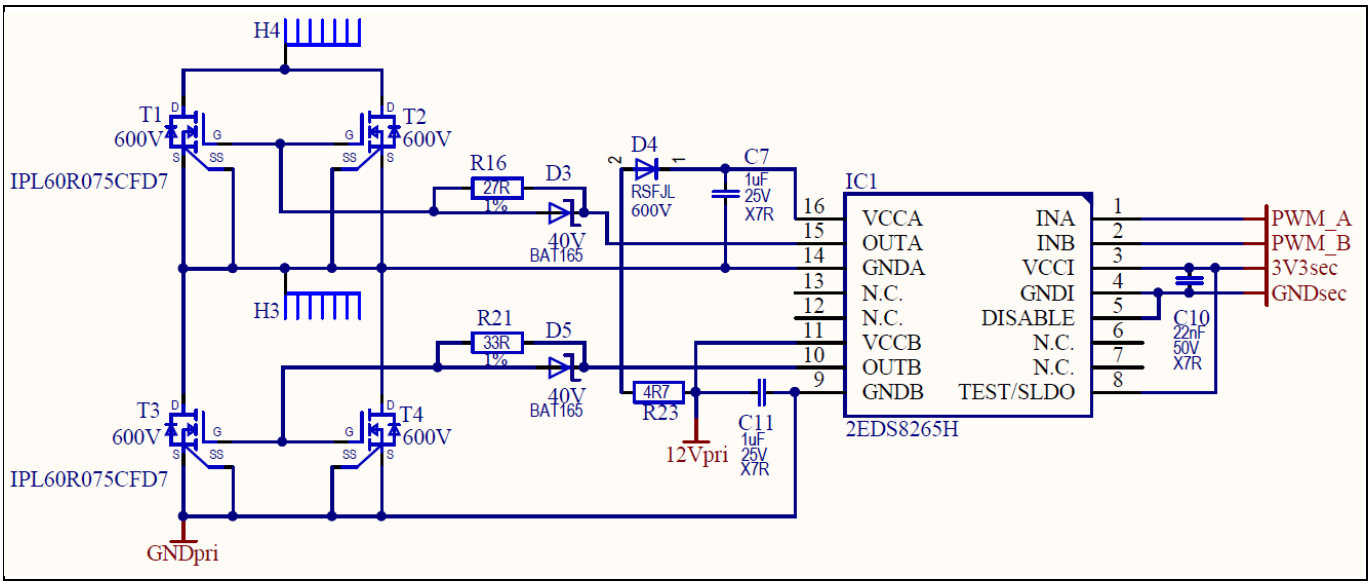

Figure 8 **Driving configuration of paralleled IPL60R075CFD7 (half-bridge schematic)**

1.3.1 CoolMOS™ CFD7 $R_{DS(on)}$ comparison

CoolMOS™ CFD7 current portfolio in SMD ThinPAK packages (Figure 9) ranges from 225 mΩ (maximum) to 60 mΩ (maximum) (best-in-class device).

600 V CoolMOS™ CFD7 SJ MOSFETs			
$R_{DS(on)}$ [Ω]	ThinPAK 8x8	$R_{DS(on)}$ [Ω]	ThinPAK 8x8
225*	IPL60R225CFD7*	115	IPL60R115CFD7
185	IPL60R185CFD7	95	IPL60R095CFD7
160	IPL60R160CFD7	75	IPL60R075CFD7
140	IPL60R140CFD7	60	IPL60R060CFD7

Figure 9 **CoolMOS™ CFD7 in ThinPAK $R_{DS(on)}$ portfolio. *Coming soon.**

For this design IPL60R075CFD7 was chosen as the best compromise between 100 percent, 50 percent and 10 percent load points performance. However, other $R_{DS(on)}$ could be used for a different distribution of losses whenever there is interest in increasing performance in certain working points of the converter.

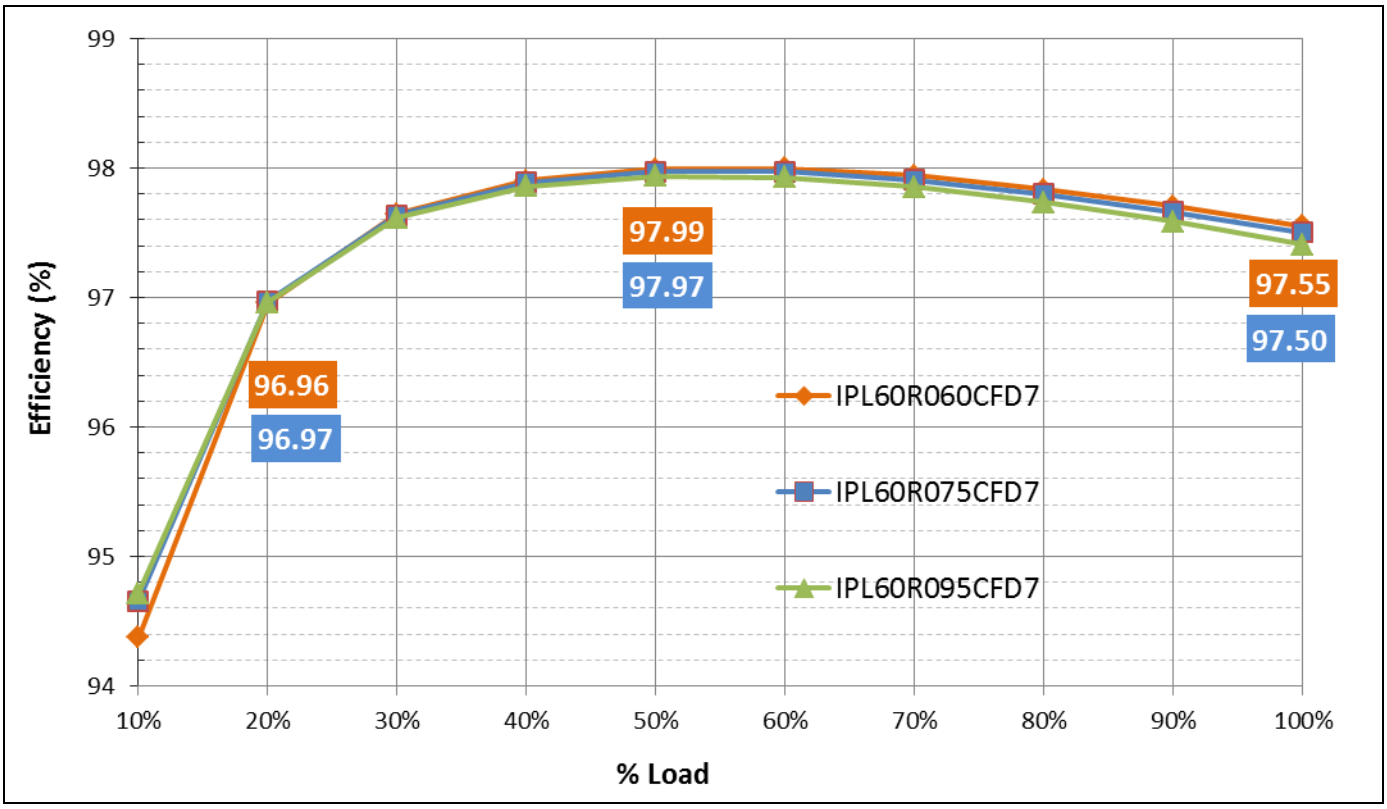

Figure 10 **Estimated efficiency of 3300 W bi-directional PSFB in buck mode with different CoolMOS™ CFD7 $R_{DS(on)}$ in ThinPAK**

As, for example, here we present an estimated performance of three different $R_{DS(on)}$ levels available in our portfolio: IPL60R075CFD7 (device currently on the design), IPL60R095CFD7 (one step higher $R_{DS(on)}$) and IPL60R060CFD7 (on step lower $R_{DS(on)}$).

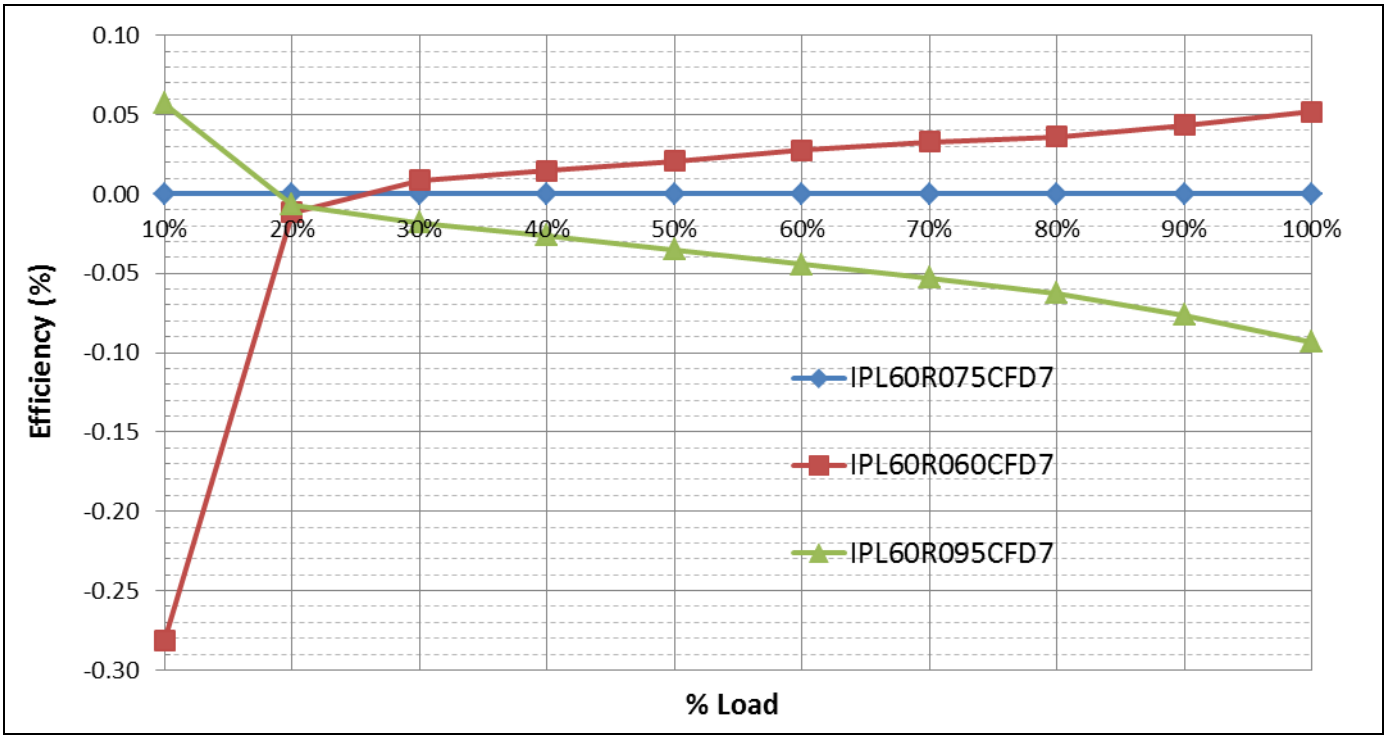

Figure 11 **Different estimated efficiencies of 3300 W bi-directional PSFB in buck mode with different CoolMOS™ CFD7 $R_{DS(on)}$ in ThinPAK**

In Figure 12 we can see the estimated losses at three main working points and how they balance for the different $R_{DS(on)}$. Althought the difference in losses at 50 percent and 10 percent is small in comparison to the difference in losses at 100 percent, the impact on efficiency is still noticeable, as seen in Figure 11.

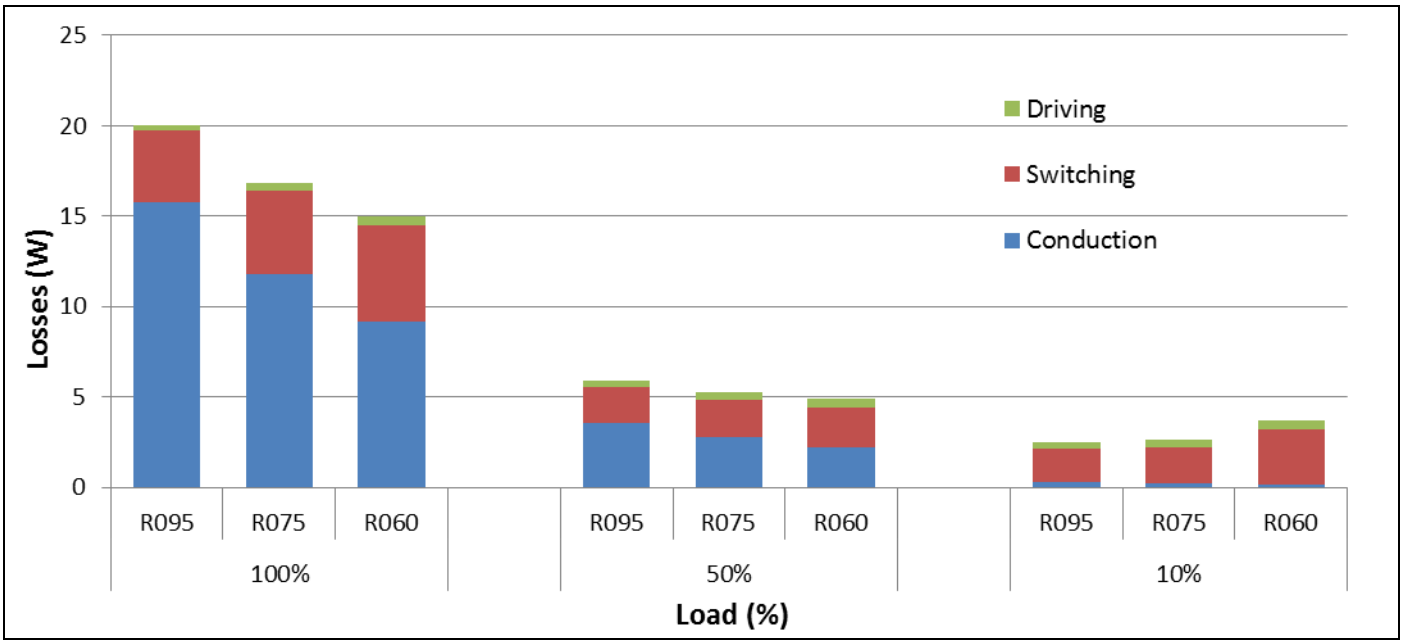

Figure 12 **Estimated distribution of losses of 3300 W bi-directional PSFB in buck mode with different CoolMOS™ CFD7 $R_{DS(on)}$ in ThinPAK**

1.3.2 CoolMOS™ CFD2 comparison

CoolMOS™ CFD2 current portfolio in SMD ThinPAK packages ranges from 725 mΩ (maximum) to 165 mΩ (maximum) (best-in-class device).

As a replacement for a fair comparison between technologies we might need to use eight times IPL65R165CFD to reach an equivalent $R_{DS(on)}$ of approximately 41 mΩ against an equivalent $R_{DS(on)}$ of approximately 37 mΩ – which we reach with IPL60R075CFD7 two times.

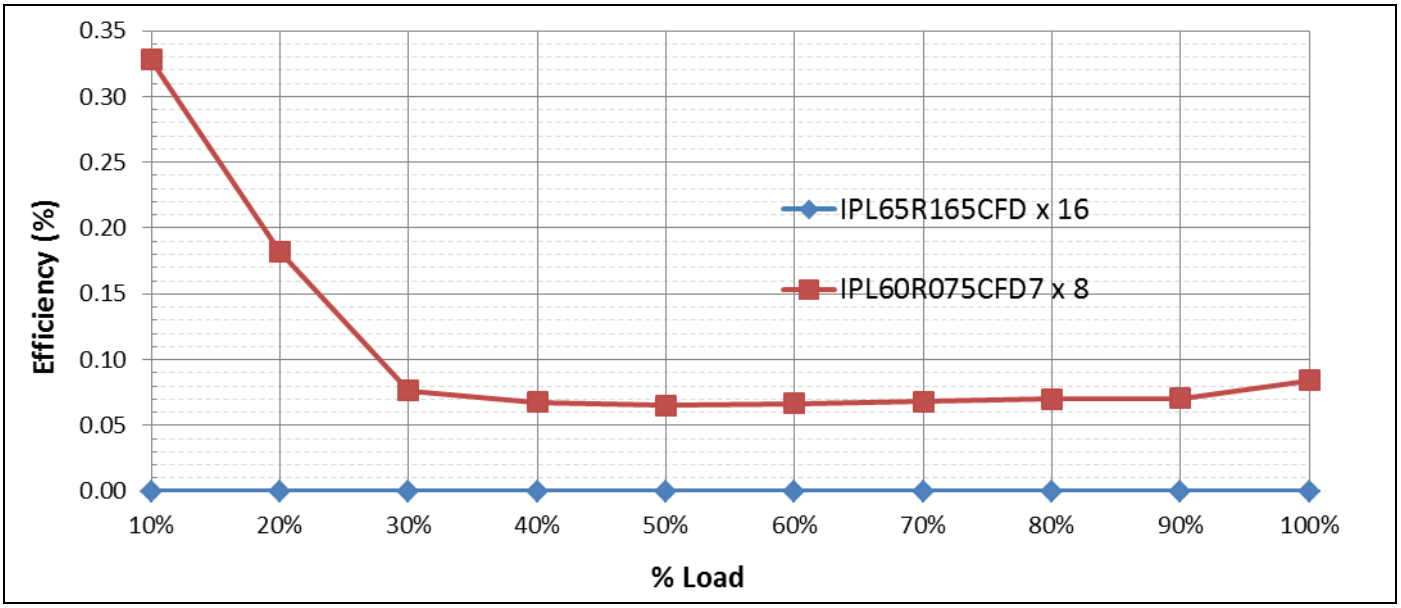

Figure 13 **Different estimated efficiencies of 3300 W bi-directional PSFB in buck mode with different CoolMOS™ fast body diode technologies**

Thanks to the Figure of Merit (FOM) of CFD7 technologies we have the benefit of lower $R_{DS(on)}$ at mid and full load wihout any compromise in switching losses at light and medium loads. Thanks to this, the converter performs better in all load ranges when comparing CFD7 against CFD2 devices (Figure 13 and Figure 14).

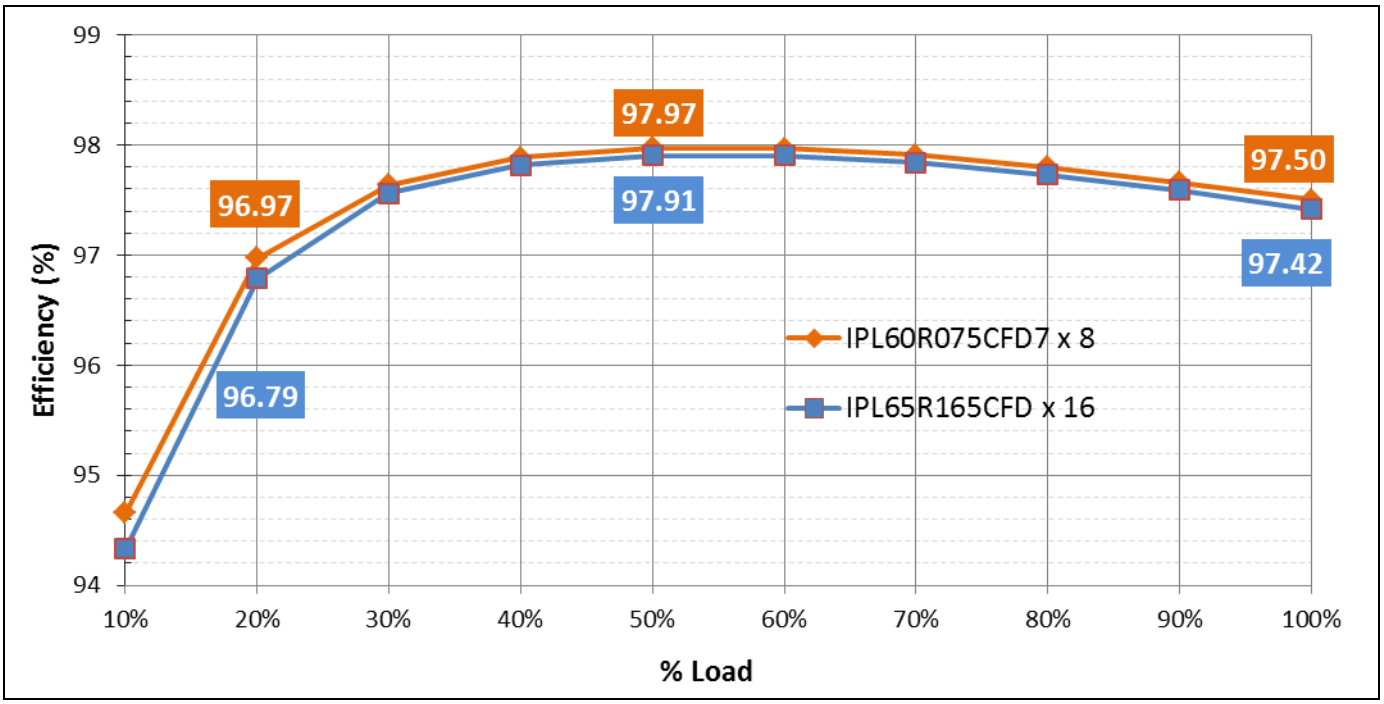

Figure 14 **Estimated efficiency of 3300 W bi-directional PSFB in buck mode with different CoolMOS™ fast body diode technologies**

In Figure 15 the distribution of losses for the main working points can be seen. The lower input and output charge of CFD7 makes it have lower switching and driving losses even when using a lower equivalent $R_{DS(on)}$.

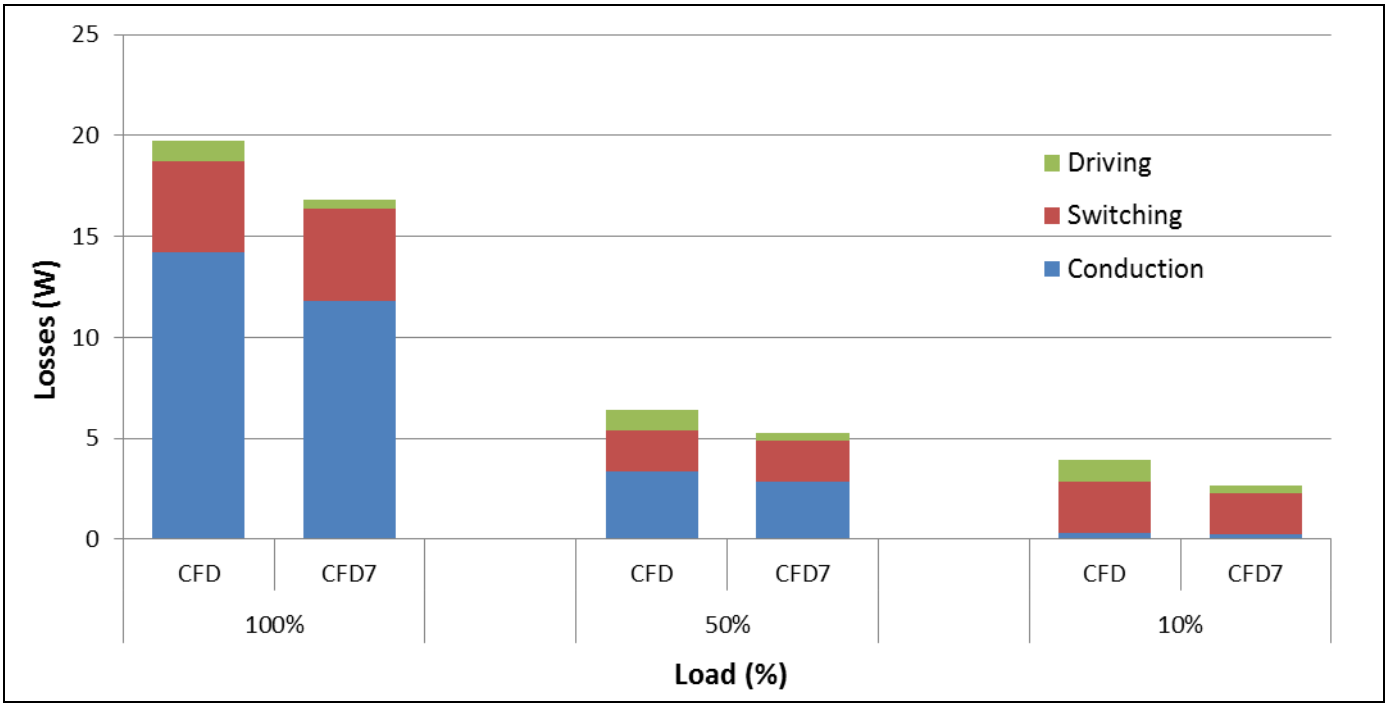

Figure 15 **Estimated distribution of losses of 3300 W bi-directional PSFB in buck mode with different CoolMOS™ fast body diode technologies**

1.4 Transformer

The main transformer has a turns ratio of 21 primary to 4 secondary, which gives 71.7 percent effective duty at nominal conditions (400 V input, 54.5 V output) or 3.59 µs at 100 kHz switching frequency.

Maximum flux peak (steady-state) is about 0.19 T, well below saturation flux density of the chosen core material: DMR95 from DMEGC manufacturer.

The transformer has a planar-like construction on PQI35/23 core geometry from DMEGC manufacturer. Primary winding has been realized with triple-insulated Litz wire of seven strands of 0.3 mm diameter from Furukawa manufacturer. Secondary winding is made of parallel tinned copper plates with a thickness of 0.6 mm.

Figure 16 shows an estimated loss distribution of the full stacked magnetic structure. Notice that the transformer core loss is nearly constant along the load (apart from the material temperature dependence) due to the nature of the converter.

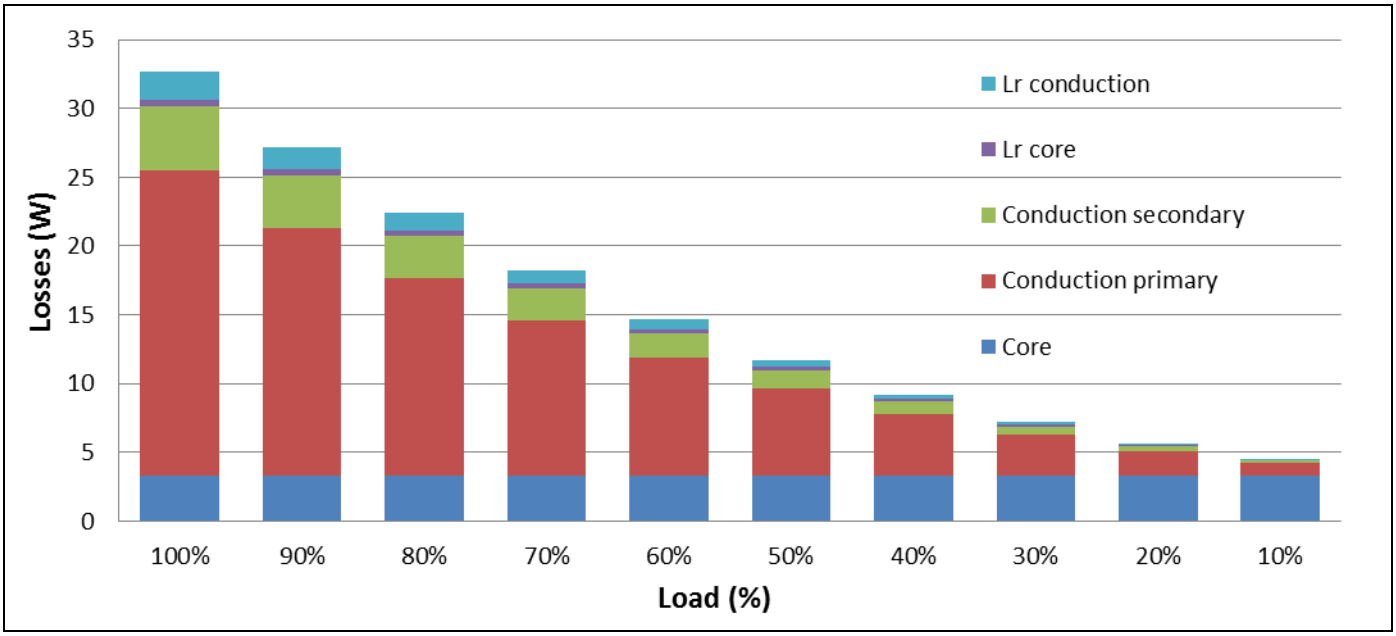

Figure 16 **Estimated distribution of losses of stacked magnetic structure: transformer and resonant inductance**

The winding technique and geometry of the core achieves good coupling (low leackage, in the order of 500 nH) with relatively low intra- and inter-winding capacitances (in comparison to a full planar realization). The inter-leaving of primary and secondary windings achieves nearly full window utilization and minimizes proximity losses (at switching frequency and higher-order harmonics, due to the nature of PSFB trapezoidal waveforms), as can be seen in Figure 17.

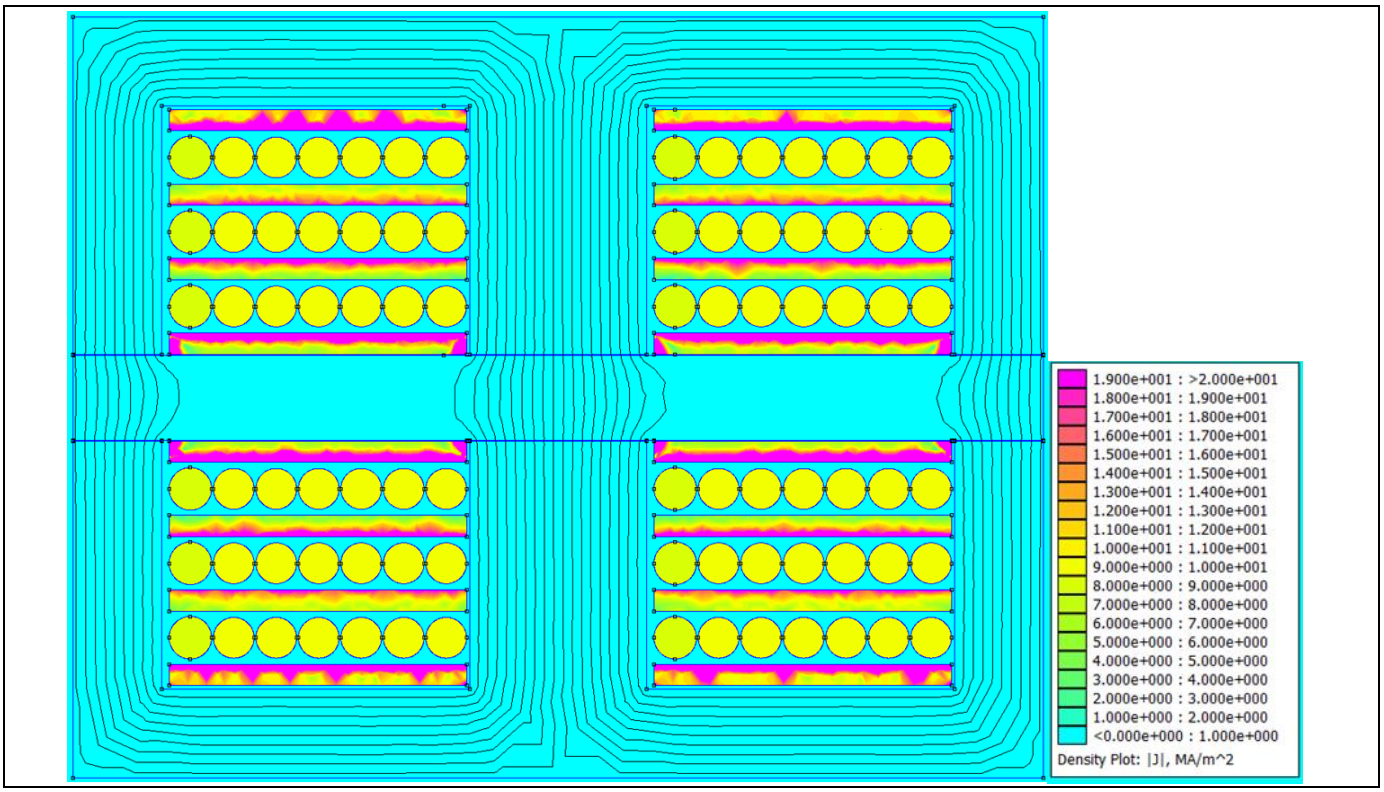

Figure 17 **Main transformer current density distribution – finite element simulation (Finite Element Method Magnetics (FEMM)**

The main transformer comprises two parallel integrated transformers. Due to the integration the flux is canceled in part of the core with a subsequent impact on the core losses (Figure 18).

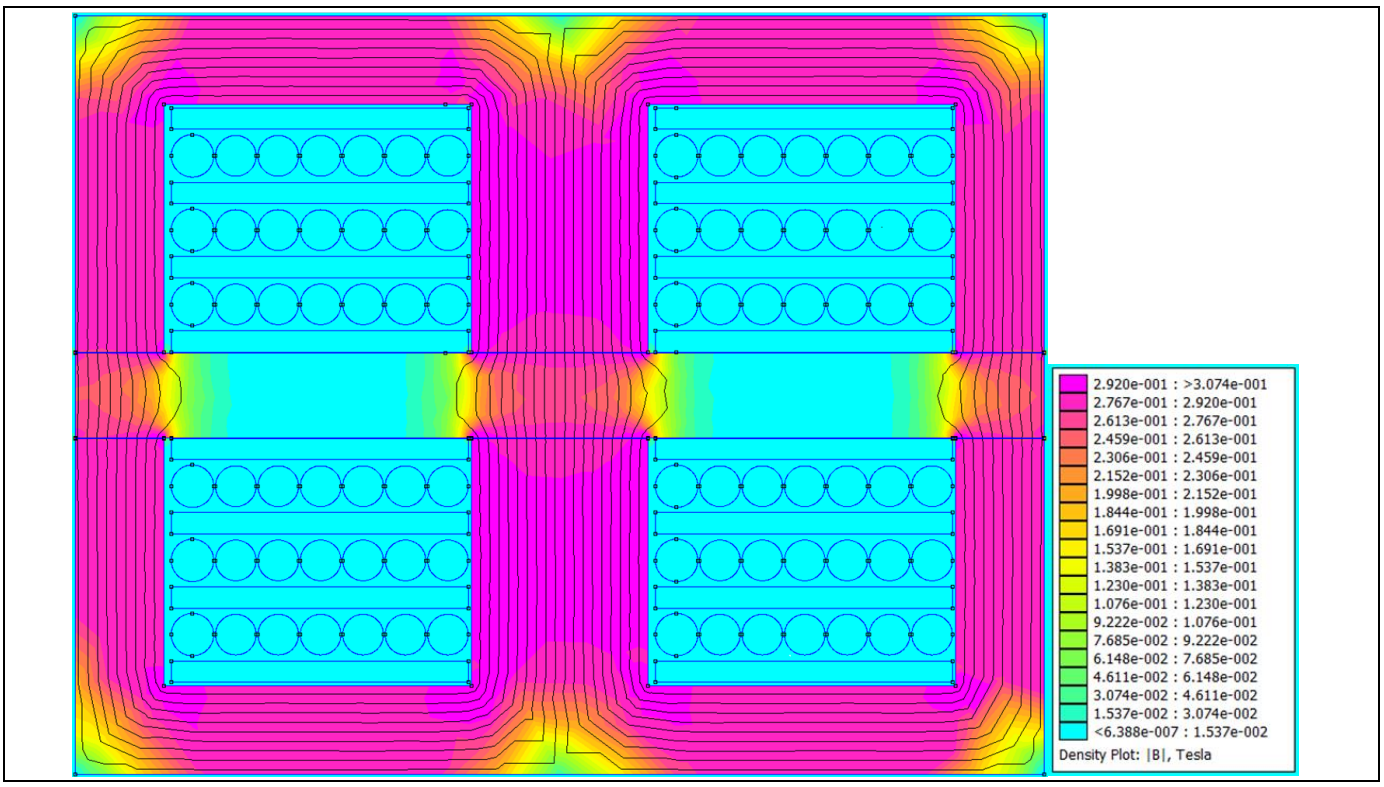

Figure 18 **Main transformer flux density distribution – FEMM**

1.5 Cooling solution

The proposed cooling solution for the full SMD design comprises a set of four copper plates for the HV bridge devices and two copper plates for the SR LV devices. The construction of the transformer, where secondary-side winding is built out of copper plates, also constitutes part of the secondary-side LV devices' heatsink.

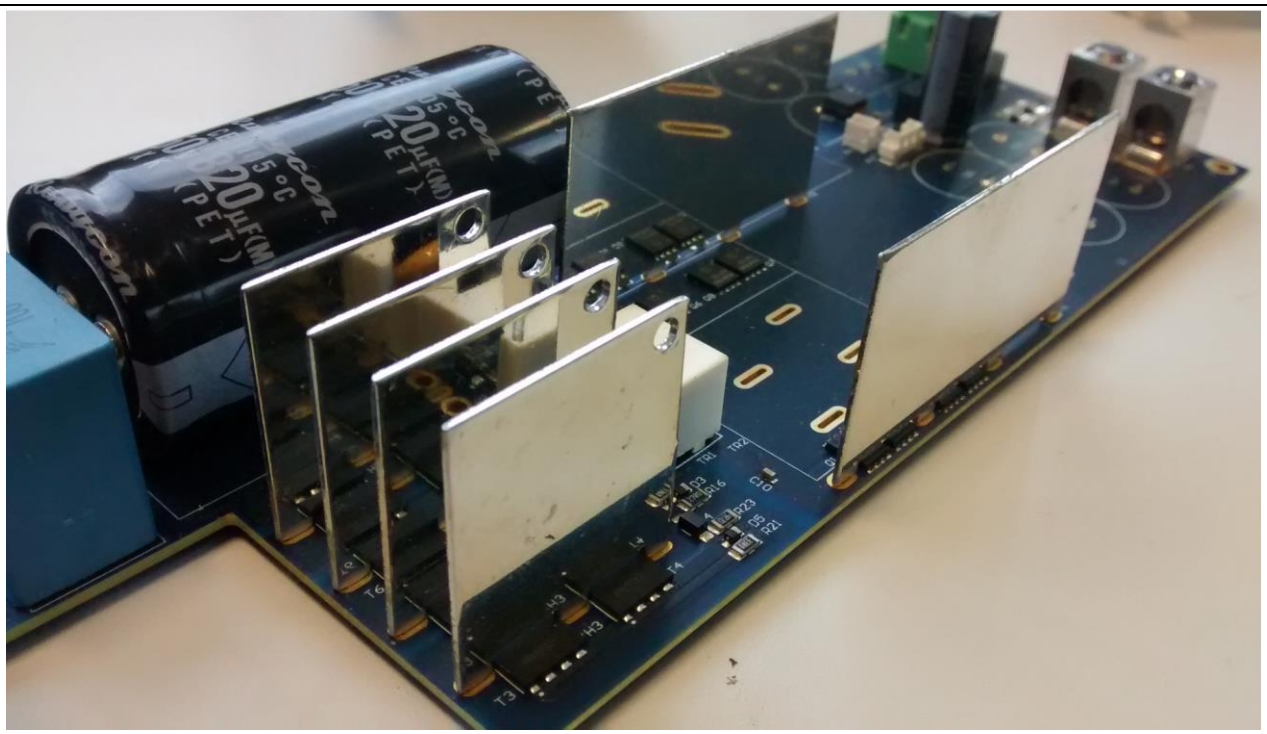

Figure 19 **Heatsinks for HV bridge devices and LV secondary devices in a partially assembled PSFB 3300 W converter board**

A single fan extracts air from the unit, which flows inunterrupted along the HV bridge heatsinks due to their construction. That keeps air pressure low and maximizes air-flow capabilities. The fan speed is modulated along the load for best efficiency (see Figure 20), as little cooling effort is required at light loads.

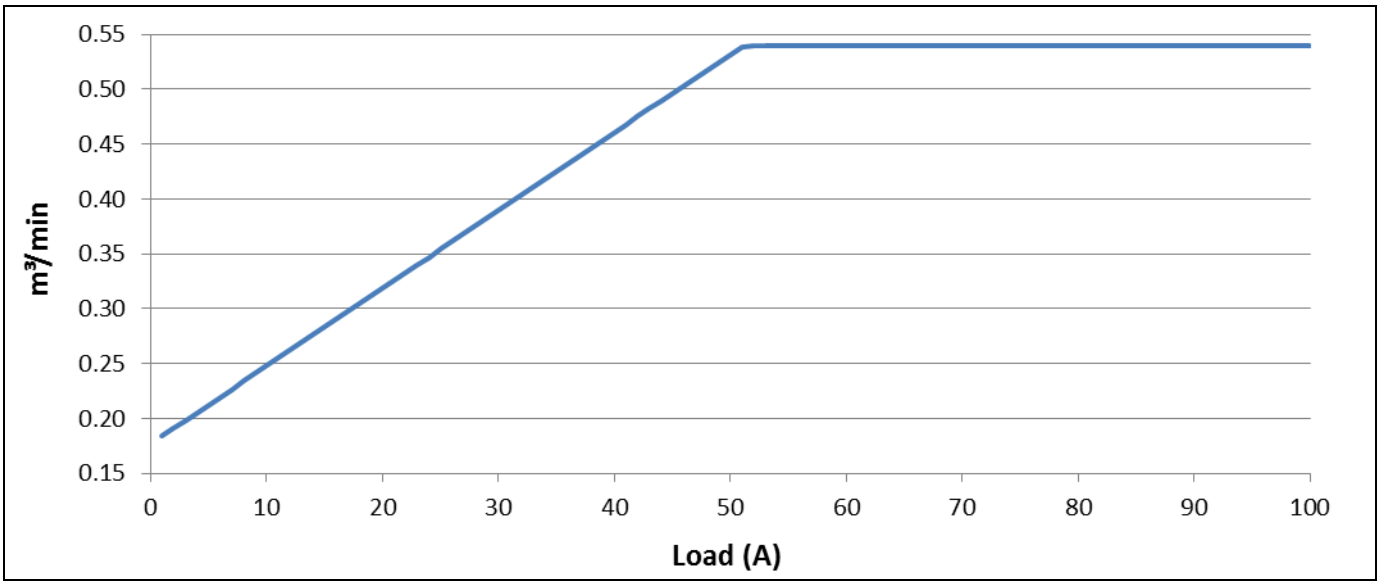

Figure 20 **Fan air-flow along converter load (assuming fan is working with low pressure)**

Based on the estimation of losses for the HV bridge devices (8 x IPL60R075CFD7), which at full load is approximately 16.4 W (considering both switching and conduction losses, but not driving, as most of the driving losses are dissipated on the external Rg and driver), some 2.05 W per device, and the measured temperature (see Figure 21) of approximately 35°C on the surface of the device packages, we can estimate thermal impedance of the proposed cooling solution in the range of 5.5°C/W from junction to air for the HV bridge devices.

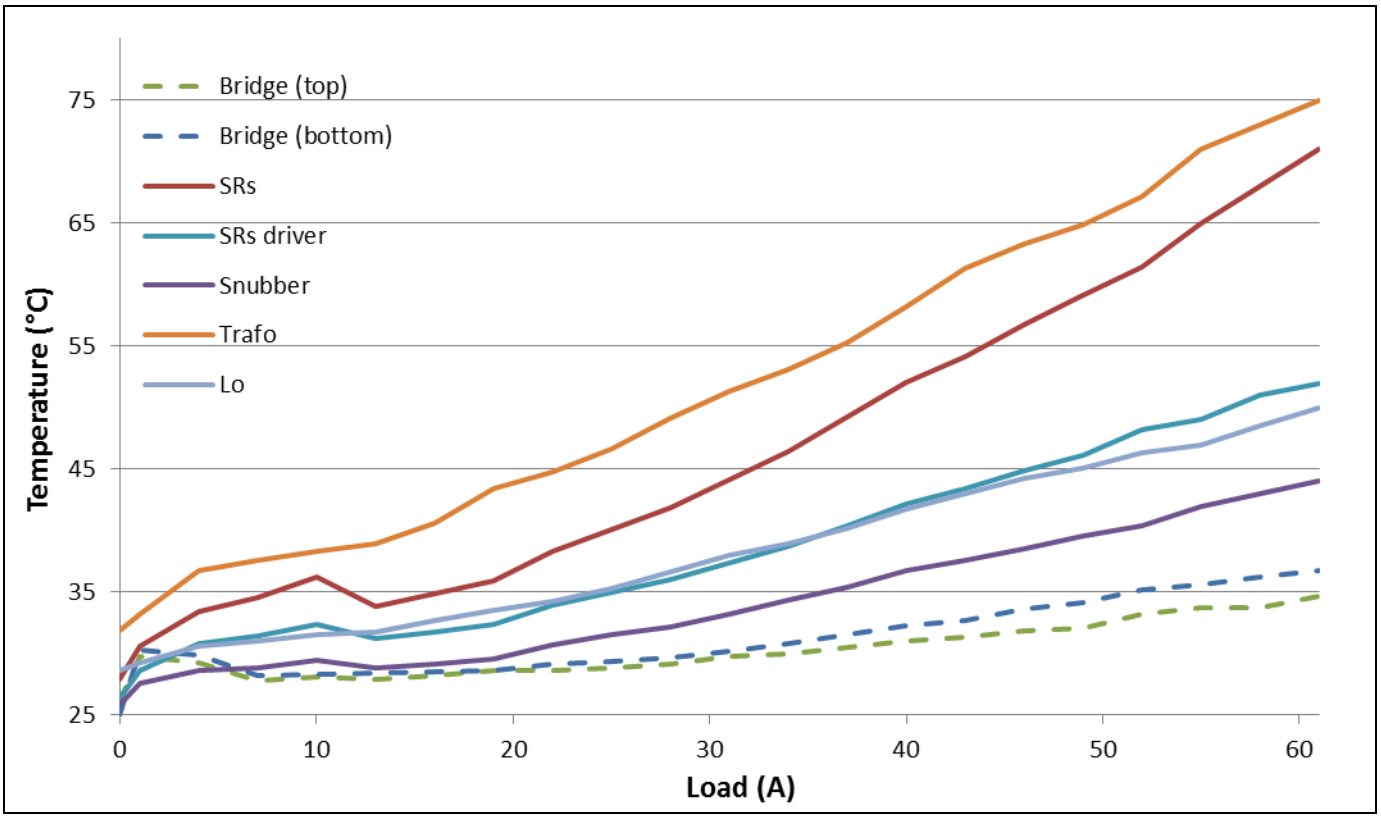

Figure 21 **Measured temperatures on PSFB 3300 W converter at 25°C room temperature and with open case**

As can be seen, the proposed cooling solution is effective, simple to manufacture and assemble, and low cost.

1.6 EiceDRIVER™ 2EDSx reinforced, 2EDFx functional isolated gate driver

The EiceDRIVER™ 2EDi is a family of fast dual-channel isolated MOSFET gate-driver ICs providing functional (2EDFx) or reinforced (2EDSx) input-to-output isolation by means of coreless transformer (CT) technology. Due to high driving current, excellent common-mode rejection and fast signal propagation, 2EDi is particularly well suited for driving medium- to high-voltage MOSFETs (CoolMOS™, OptiMOS™) in fast-switching power systems with following features.

- 4A / 8 A or 1A / 2A source / sink output current

The low-ohmic output stage of the EiceDRIVER™ family allows, in this topology, the fast turn-on and turn-off of the HV bridge CoolMOS™ (two in parallel) with the best class low source resistance (0.85 Ω for 4A source current) and sink resistance (0.35 Ω for 8A sink current) of isolated gate driver.

- PWM signal propagation delay typ. 37ns with 3ns channel-to-channel mismatch and +7/-6 ns propagation delay variance

The isolated gate driver 2EDS8265H and 2EDF7275F provide typical 37ns propagation delay with an input filter internally in order to attenuate the noise with pulse width below 18ns. The best class of +7/-6 ns propagation delay accuracy assures the tight delay window for designers. Meanwhile the designer can benefit from maximum 3 ns channel to channel mismatch in half bridge design or driving parallel MOSFETs.

• Common Mode Transient Immunity (CMTI) >150V/ns

The CMTI indicates the robustness of the IC to fast voltage transients (dV/dt) between its two isolated grounds; the dV/dt causes a current flow through the parasitic input-to-output (C_{IO}) capacitance of the IC corrupting the transmitted gate signal. The isolated EiceDRIVER™, thanks to the CT technology, show a robust CMTI (greater than 150V/ns) compared to the gate transformer.

• Fast safety turn-off in case of input side Undervoltage Lockout (UVLO)

The 8V UVLO for the 2EDS8265H and 4V UVLO for the 2EDF7275F well suits the transfer characteristic of the HV IPL60R075CFD7 and LV BSC093N15NS. In general, 8V UVLO fits for complete CoolMOS™ and normal level OptiMOS™ and 4V UVLO fits for logic level OptiMOS™ products to keep safe operation and turn-off in case of gate driver supply drop off.

2EDFx for functional isolation is typically used as a primary-side controlled galvanically isolated driver. 2EDSx for reinforced safe isolation is typically used as a secondary-side controlled isolated gate driver.

Among the possible benefits of using an isolated gate driver in comparison to a gate driver transformer:

- Increase of power density. A gate driver transformer design may include a driver and additionally a transformer, with the transformer already occupying more space than an isolated driver.
- Duty cycle capability. Transformer solutions are limited in their duty cycle capability as the core needs to be reset every cycle to avoid saturation.This in principle is not an issue for this topology. However in special conditions and depending on how the controller handles them it could be seen that a pulse much longer than the steady-state pulse is applied (load jump) or several pulses are applied to the same gate output in a sequence, not letting the core reset properly (see burst in Figure 23).
  EiceDRIVER™ isolated can handle those special conditions without problem (see burst in Figure 23) and large or small duty cycles as long as the high-side driver output is properly supplied.
- Driving frequency capability. On the same principle as the previous point, gate driver solutions cannot handle switching frequencies low enough to cause core saturation. Low switching frequencies involve bigger cores and again power density decrease. EiceDRIVER™ isolated can handle a wide range of switching frequencies and could be adapted in later stages of a design without problem (a gate driver solution may need to be replaced by a bigger core).

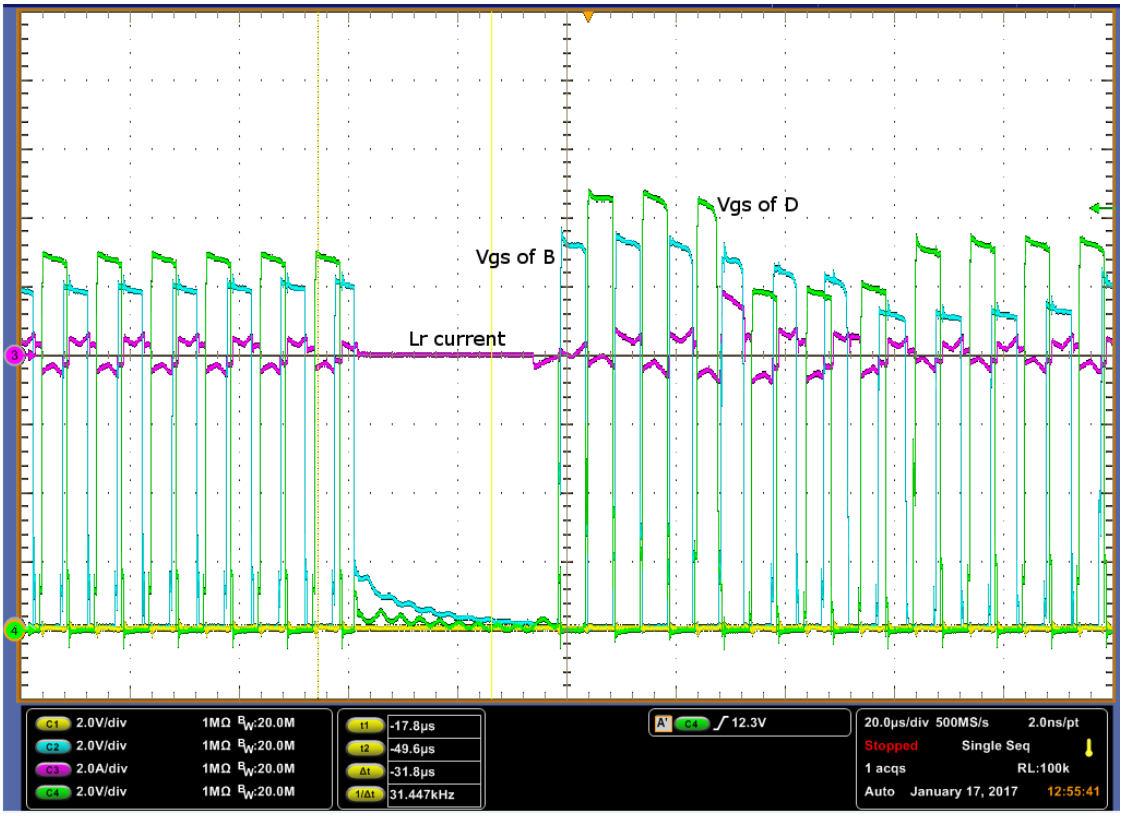

Figure 22 **Burst mode operation with gate driver transformer. After the controller resumes driving pulses it could be seen as a distortion of the output of the transformer due to slight saturation of the core.**

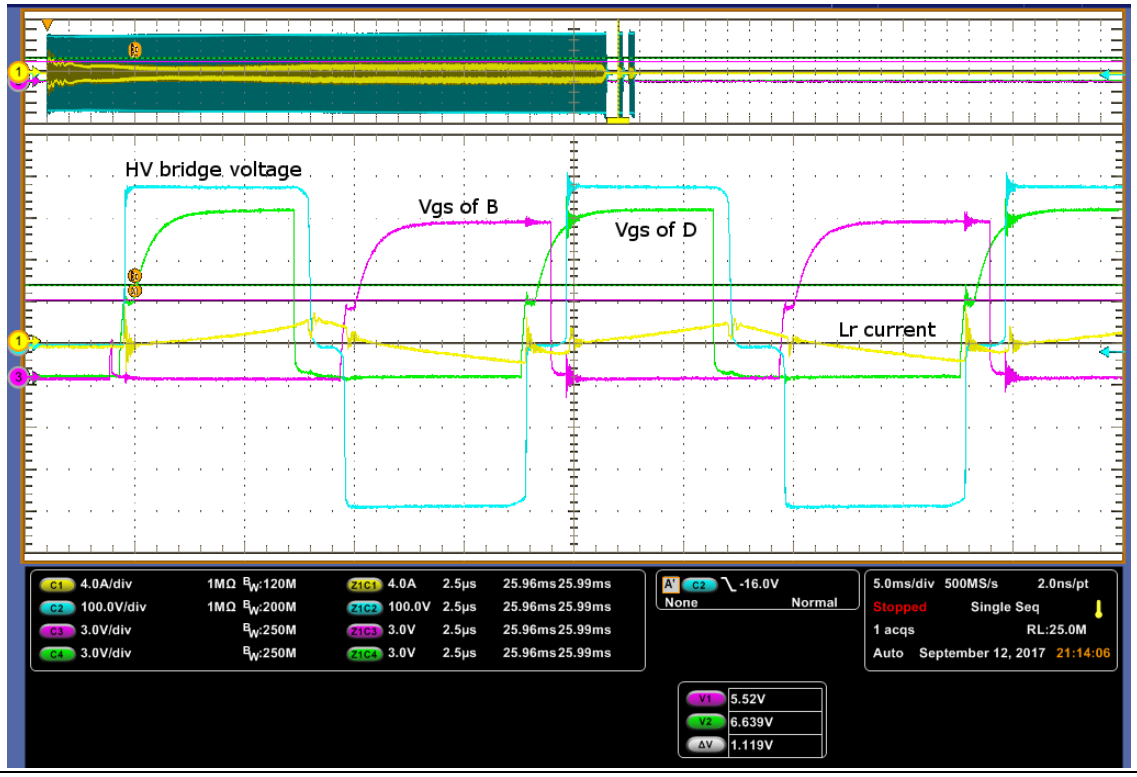

Figure 23 **Burst mode operation with EiceDRIVER™ reinforced isolated driver. The controller resumes switching with normal steady-state pulses at the output.**

1.7 Validation set-up

The 3300 W bi-directional PSFB can operate as an isolated buck or as an isolated boost converter, with the power flowing from the HV rail to the isolated LV rail or vice versa.

1.7.1 Buck mode

For validation of the buck mode the suggested set-up includes:

- HV supply capable of 400 V and at least 3400 W (when testing up to full load)
- LV electronic load (0 V to 60 V), in constant current mode, capable of at least 3300 W (when testing up to full load)

Nominal input voltage of the converter is 400 V. The converter starts to operate at 375 V with a hysteresis window up to 415 V and down to 350 V, as indicated in Figure 24.

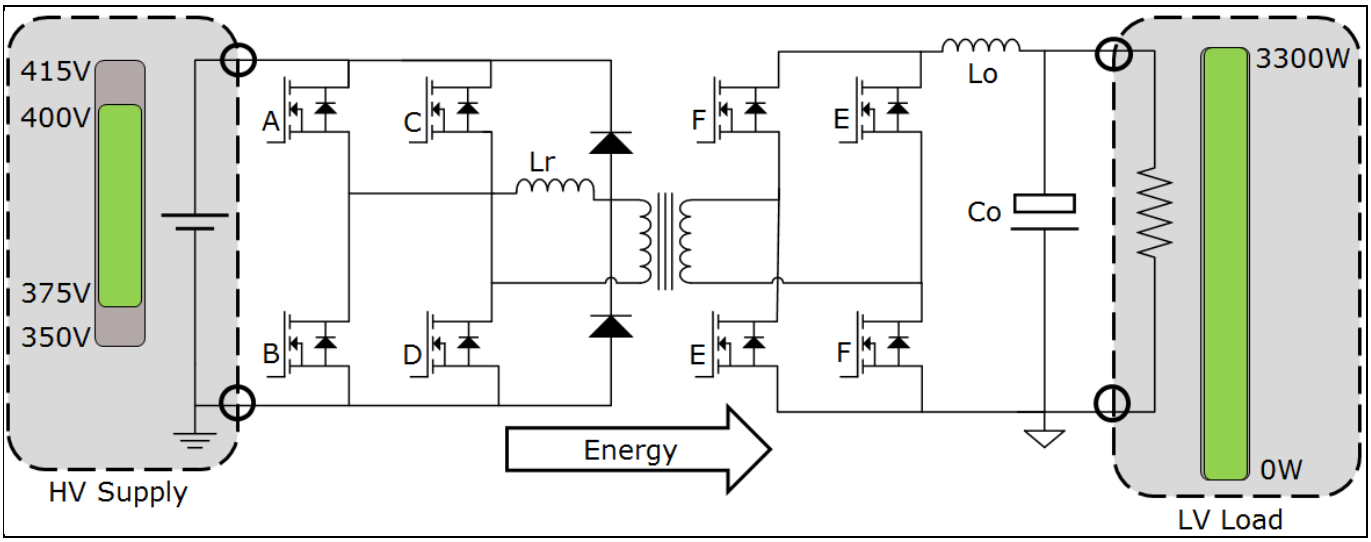

Figure 24 Buck mode recommended validation set-up

1.7.2 Boost mode

For validation of the boost mode the suggested set-up includes:

- HV supply capable of 330 V to 380 V and at least 1 A (pre-charging of bulk capacitor)
- HV electronic load (0 V to 400 V), in constant current mode, capable of at least 2400 W (when testing up to full load)
- LV supply capable of 0 V to 58 V and at least 2500 W (when testing up to full load)

A HV diode might be placed between the HV supply and the HV load as in Figure 25 to decouple the HV supply once the 3300 W PSFB converter starts up.

The converter requires both the HV and the LV side voltages to be within the ranges in Figure 25 for starting up (the order is irrelevant).

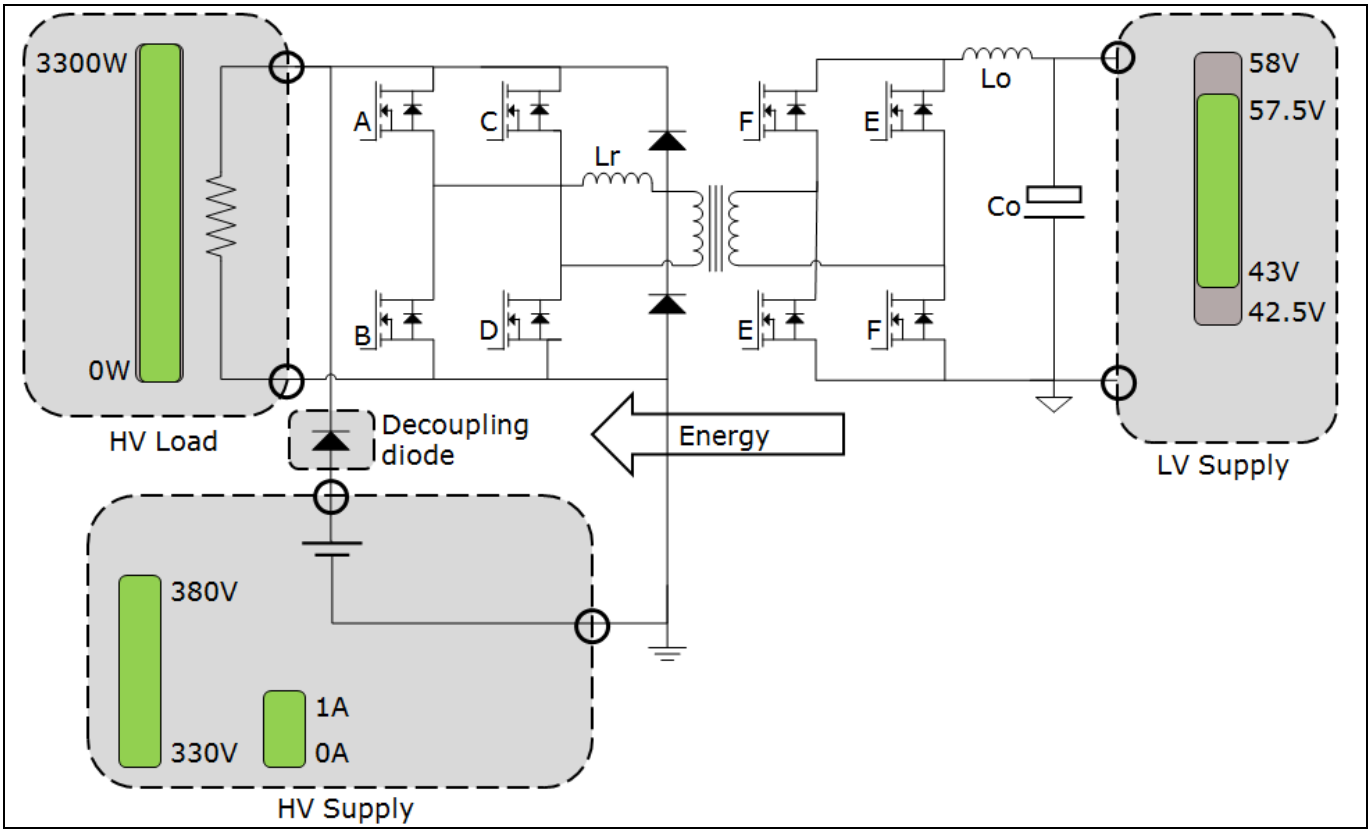

Figure 25 **Boost mode recommended validation set-up**

Note: *The buck and boost validation set-ups could be combined with an additional diode decoupling the LV supply. However, when doing so, all the current in any of the directions of flow would be passing through one of the decoupling diodes, wich may require appropiate cooling.*

2 Buck mode results

2.1 Specification and test results

This chapter presents the specifications, performance and behavior of the 3300 W bi-directional PSFB with CoolMOS™ CFD7. Table 1 shows the demonstrator performance and specifications under several steady-state and dynamic conditions.

Table 1 Summary of specifications and test conditions for the 3300 W bi-directional PSFB

Test	Conditions	Specification
Efficiency test	380 V input, 54.5 V output	η_{pk} = 98 percent at 1500 W (50 percent load)
Output voltage		60 V to 40 V
Steady-state V_{out} ripple	380 V input, 54.5 V output	$\lvert\Delta V_{out}\rvert$ less than 200 mV_{pk-pk}
Brown-out		370 V on to 350 V off 415V off to 390 V on
Load transient	5 A ↔ 31 A, 0.5 A/µs	$\lvert\Delta V_{out}\rvert$ less than 450 mV_{pk}
	31 A ↔ 61 A, 0.5 A/µs	
OCP	5 min. at 77 A to 83 A	Shut down and resume after 5 min.
	1 ms at 83 A to 85 A	
	20 µs at 85 A	Shut down and latch
	Output terminals in short-circuit	Detection within switching cycle Shut down and latch

2.2 Performance and steady-state waveforms

2.2.1 HV full-bridge

The low E_{oss} energy of IPL60R075CFD7 results in full ZVS of the lagging leg (switches C, D) down to no load and partial ZVS of the leading leg (switches A, B) in light-load conditions (Figure 26), with full ZVS at 20 percent load and above.

With partial ZVS only a small part of the E_{oss} is lost, and as a result switching losses of CFD7 are low at any load conditions and the overall loss contribution along all load ranges of the converter is also relatively low (Figure 6 and Figure 7).

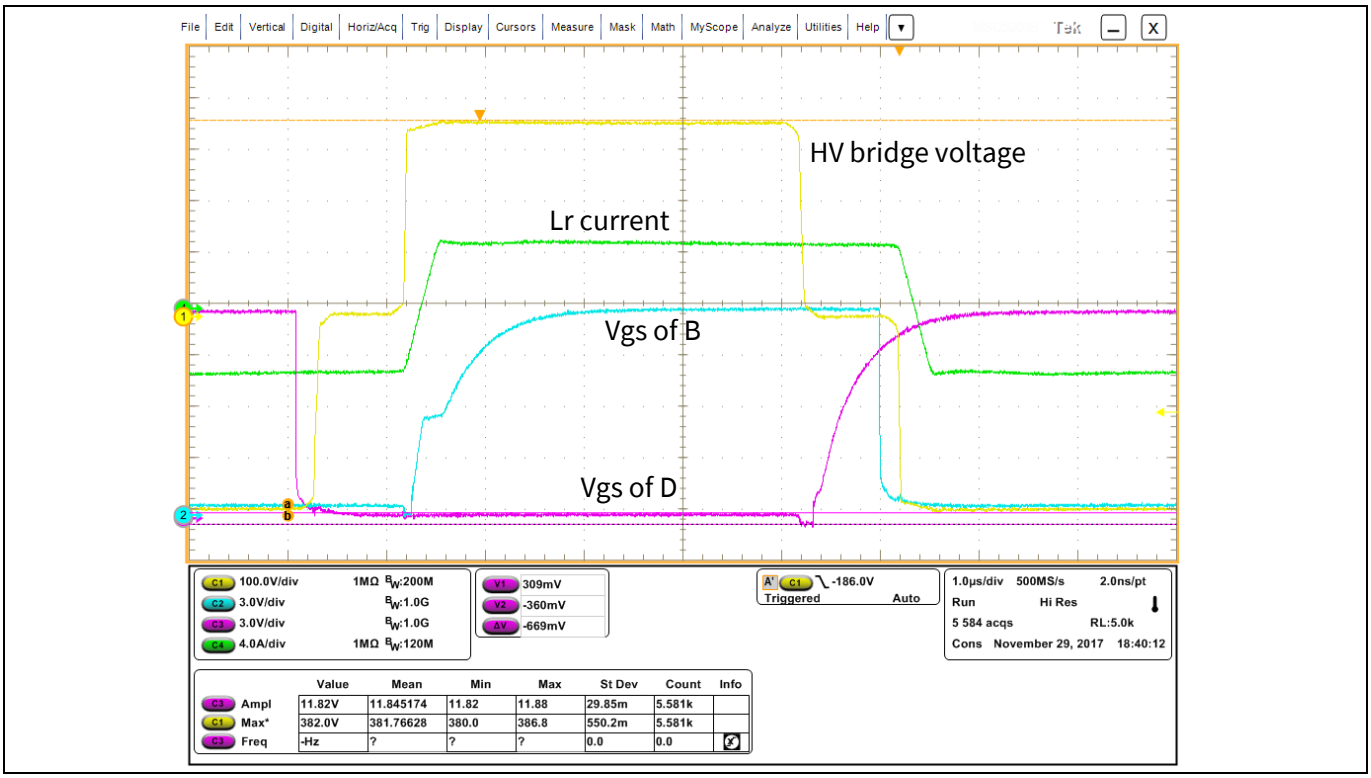

Figure 26 **ZVS turn-on of lagging leg (D switch) and partially hard-switched turn-on of leading leg (B switch)**

An additional benefit of the low E_{OSS} energy and having near-ZVS transition at no load is the lower dv/dt values and lower or no-drain voltage overshoot of the HV MOSFETs due to the smooth QR transitions (better EMI).

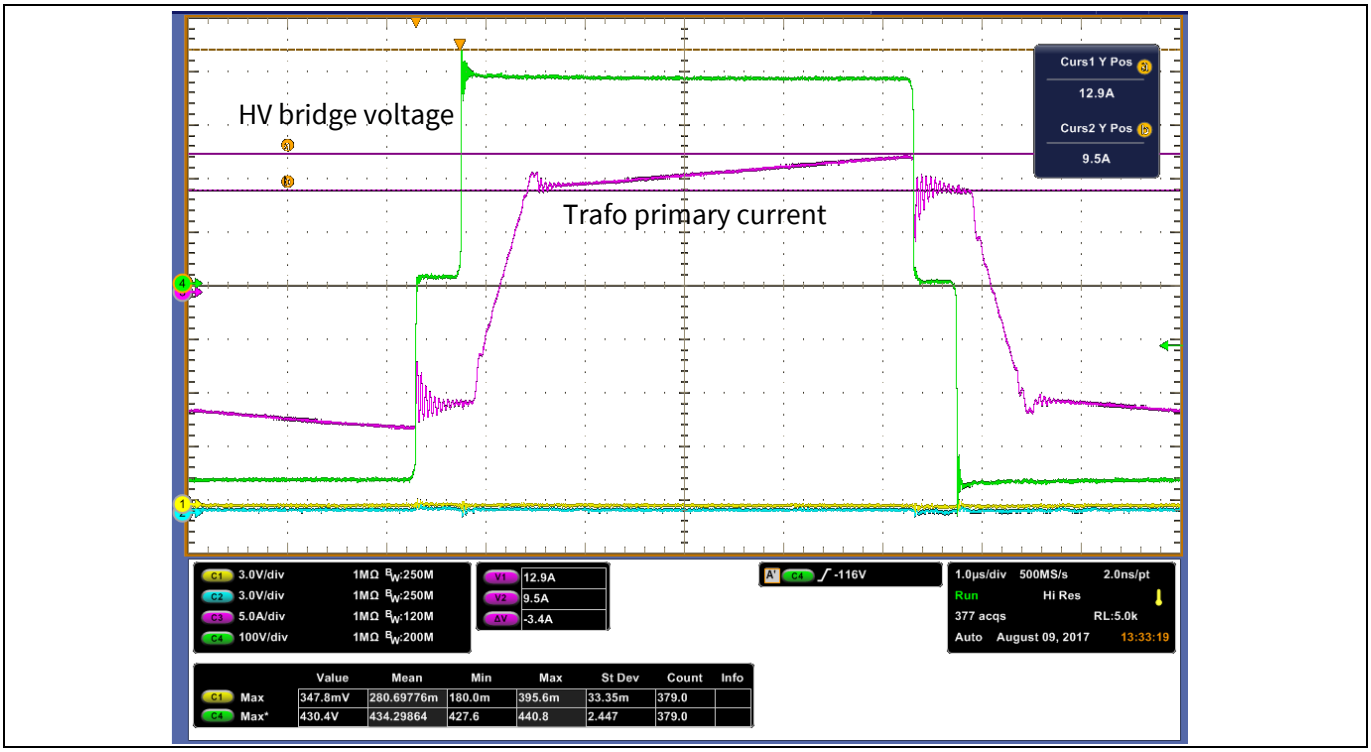

Figure 27 **Full-load drain voltage of bridge overshoot**

The highest drain voltage overshoot in the HV MOSFETs happens at full load (Figure 27), due to relatively high current hard-switched turn-off transition. In these transitions the parasitic inductances of the MOSFET package and the layout induces a di/dt voltage overshoot.

However, thanks to the low inductances of Infineon's ThinPAK package the overshoot is well under the derated maximum voltage (430 V in Figure 27 for an allowed maximum of 480 V, 80 percent derating of 600 V).

2.2.2 Synchronous rectifiers

The rectifying stage has a full-bridge configuration with 16 pieces of 9.3 mΩ 150 V OptiMOS™ 5 in Super SO-8 package.

With 16 packages the dissipated power can be better spread, bringing higher cooling capability and performance (lower $R_{DS(on)}$ increase due to temperature).

The full-bridge configuration allows the usage of the 150 V voltage class with more than enough margin for the maximum drain voltage overshoot (90.88 V in Figure 28 for an allowed maximum of 120 V, 80 percent derated of 150 V).

The controller adapts the turning-on and turning-off points of the synchronous rectifiers along the load for a minimum body diode conduction time in order to reduce conduction losses and reduce generation of reverse recovery charges (Qrr) (better efficiency and lower drain voltage overshoot).

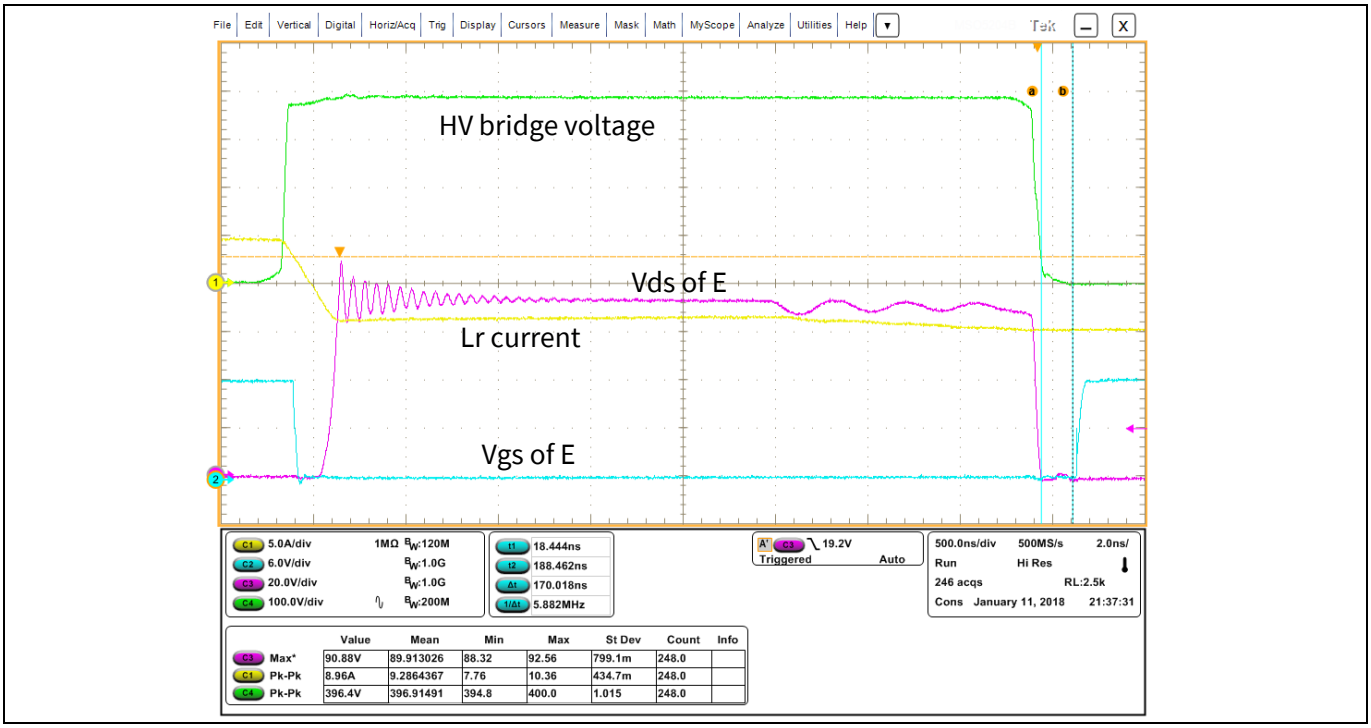

Figure 28 Standard SR driving mode

2.2.3 Dynamic response

The controller implements peak current control mode with software fixed point compensation network designed for a bandwith of 3.51 kHz with a phase margin of 53.9 degrees and 15 dB gain margin, well within standard stability criteria requirements.

The dynamic response to load jumps (Figure 29) correlates well to the expected response of the designed compensation network, with an overshoot and undershoot within 1 percent of the nominal output voltage for a 50 percent load jump.

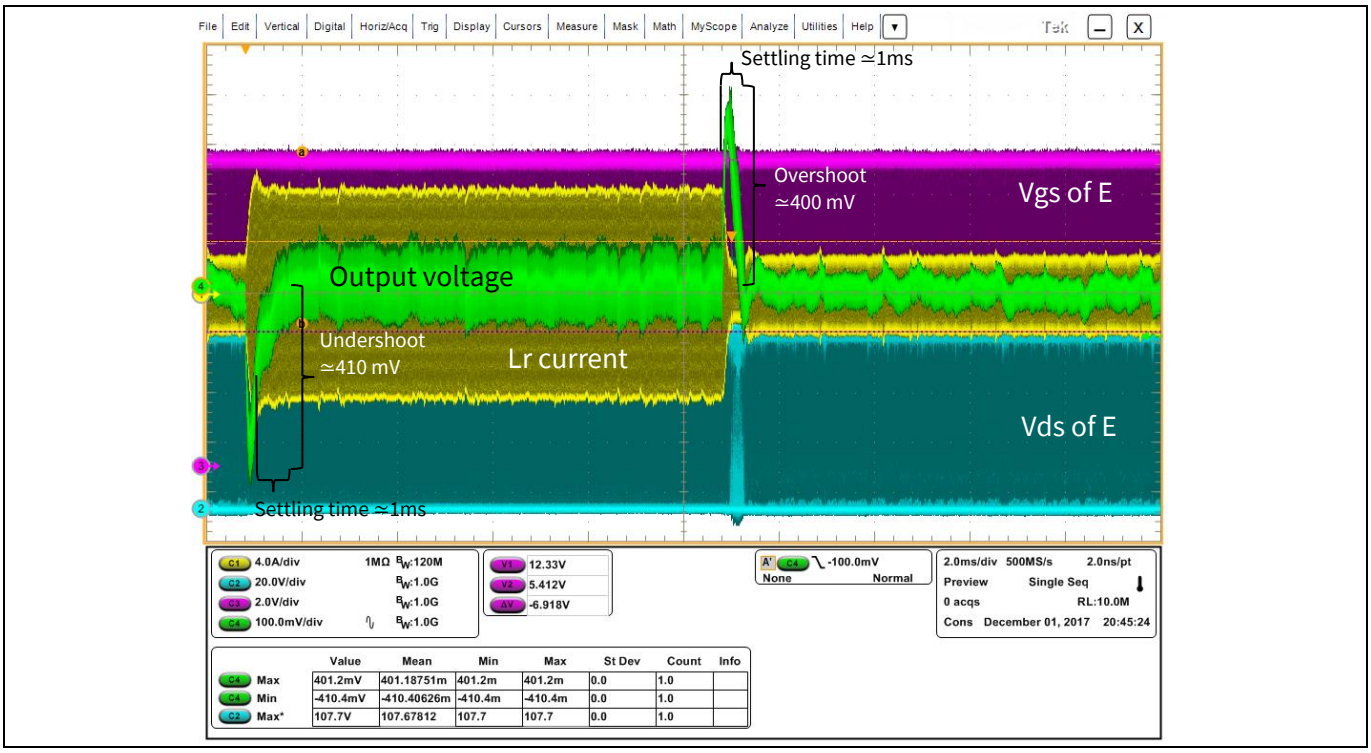

Figure 29 Load-jump, half to light load and light to half load

2.2.4 Start-up

The controller implements a soft-start sequence to ensure the converter powers up with minimal stress over any of the components.

In the starting up sequence the output voltage is ramped up in close loop operation. The controller increments the output voltage reference within a timed sequence (Figure 30).

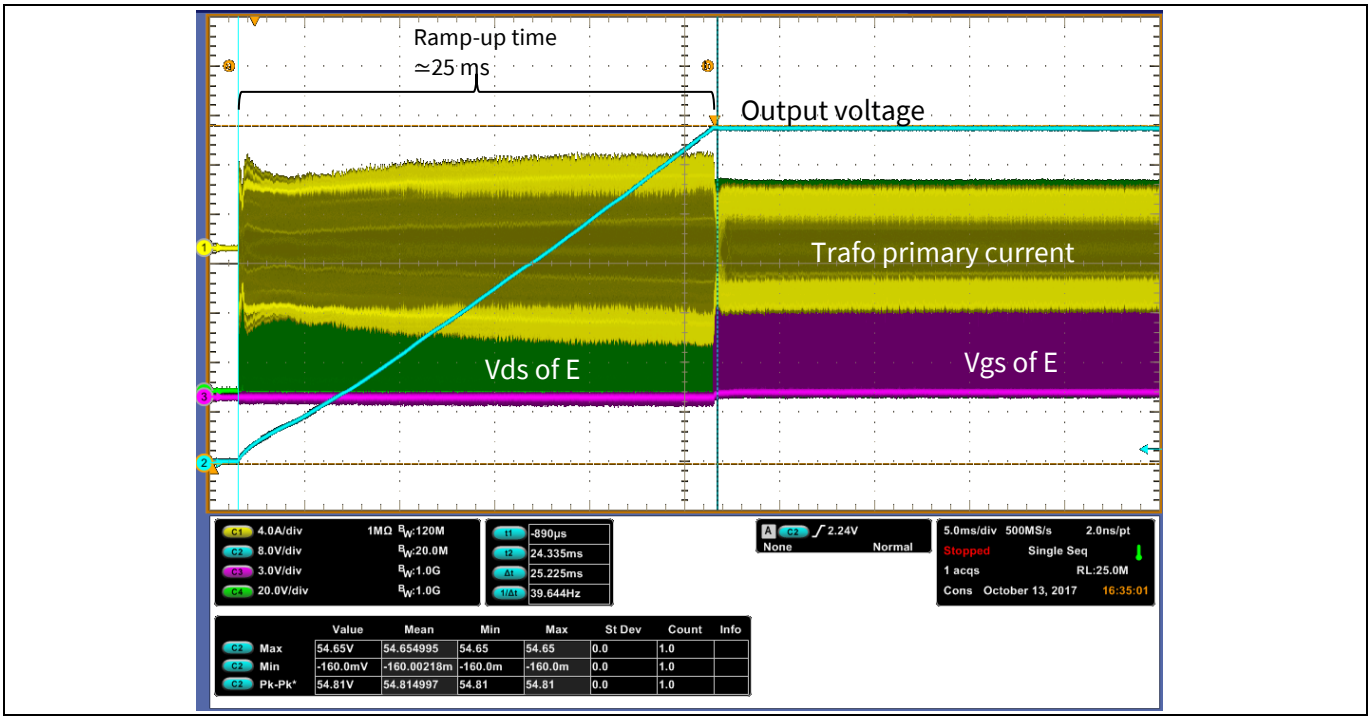

Figure 30 Output voltage soft-start-up

2.2.5 Burst mode

For further reduction of power losses under light-load conditions (less than or equal to 8 percent load) the controller uses burst mode.

The implemented burst mode ensures that under any condition the HV MOSFETs operate under full or partial ZVS (Figure 31), which reduces the power loss and maintains the smooth QR transitions of the drain voltage (little or no overshoots and better EMI).

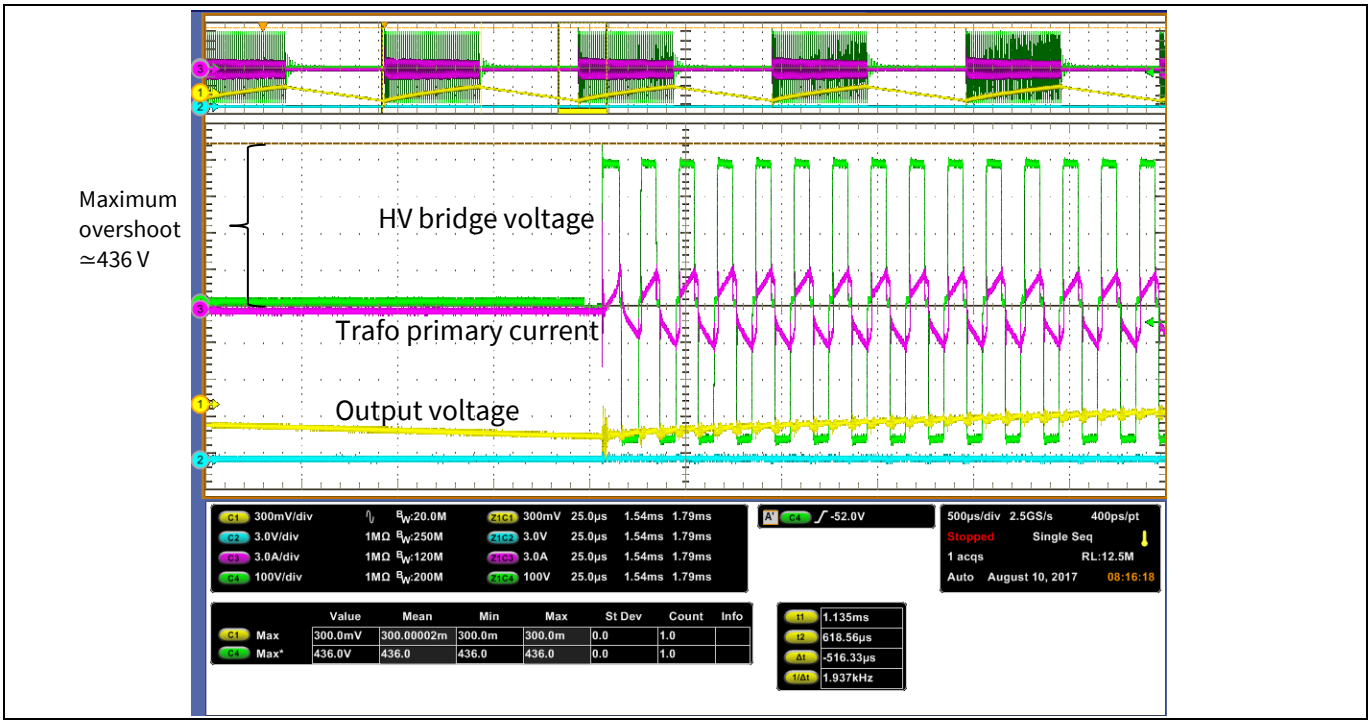

Figure 31 **Burst – output voltage (yellow), transformer primary current (pink), bridge voltage (green)**

2.2.6 Constant power limitation

The controller includes a constant power limitation curve (Figure 32), which decreases the output voltage when the output current goes above 61 A nominal to maintain the maximum 3300 W output power.

Up to 73 A and 45 V output the converter may operate steadily. If the current increases further, up to 83 A and 40 V output, the converter would operate up to 5 minutes before shuting down as thermal protection. The converter will revert to a normal state after an additional 5 minutes.

A hard limit of 85 A output will shut down the converter and latch (considered as short-circuit).

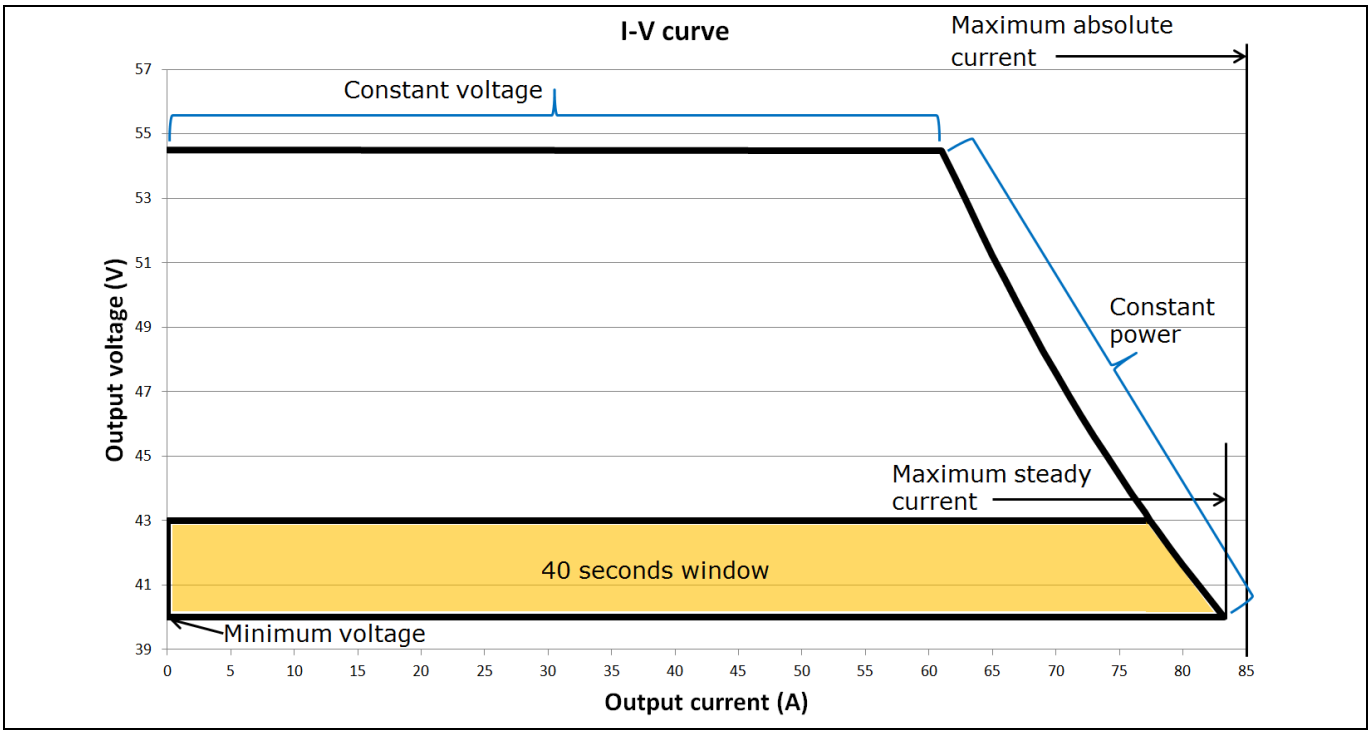

Figure 32 Constant voltage, constant power curves

The output current measurement shunt is the cause of the output voltage droop along the load in Figure 32.

2.3 Thermal map

The converter is designed to run enclosed in a cover for the fan to provide enough air-flow by the channeling effect.

The thermal captures in Figure 33 and Figure 34 have been taken with the converter running without enclosure for illustrative purposes (enclosed temperature values would be lower).

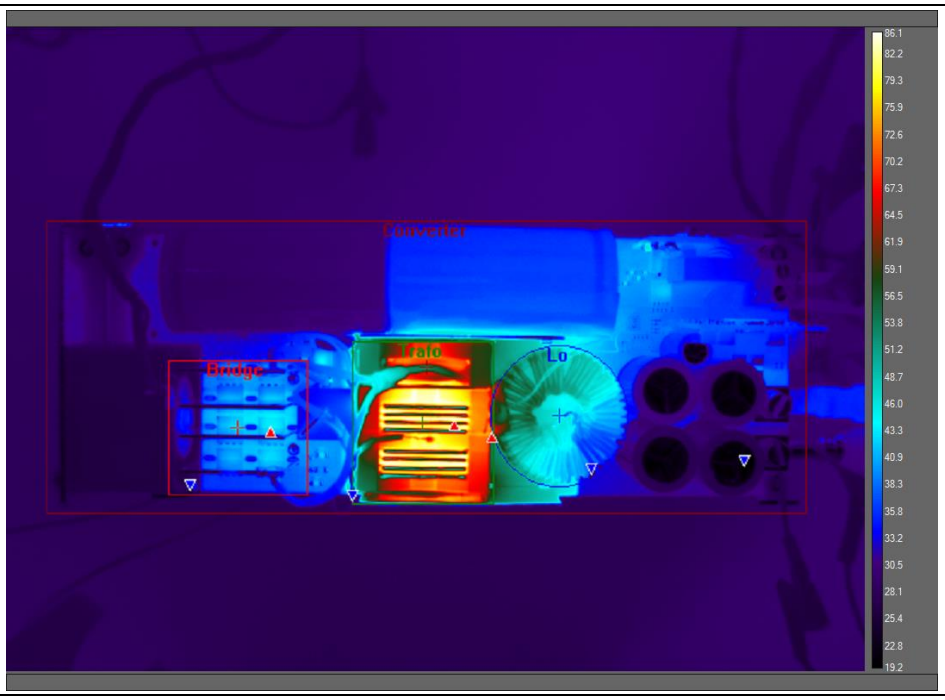

Figure 33 Thermal capture at 61 A load with open case and external fan – front view

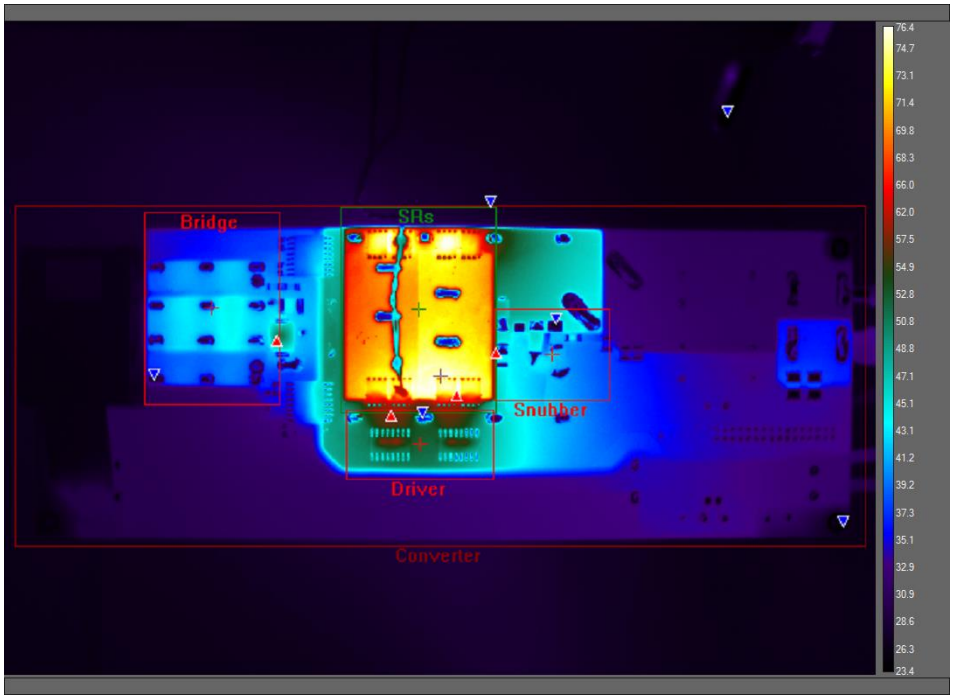

Figure 34 **Thermal capture at 61 A load with open case and external fan – bottom view**

3 Boost

3.1 Operation

In boost mode the 3300 W bi-directional PSFB behaves as an isolated boost converter.

The output filter choke (Lo) becomes the boost inductor.

The SR MOSFETs behave as the boost switch: short-circuiting Lo between the LV supply and ground to store energy or letting the stored energy flow to the HV rail through the isolation transformer. In Figure 35, enclosed between the vertical markers *a* and *b*, is the effective boost duty cycle.

The HV bridge behaves in this mode as the boost diode. The HV bridge is actively driven to provide synchronous rectification and reduce drain voltage overshoot in the LV MOSFETs when working in this mode.

Note: The modulation scheme for the operation of a PSFB as a bi-directional converter is registered and pending patent by Infineon.

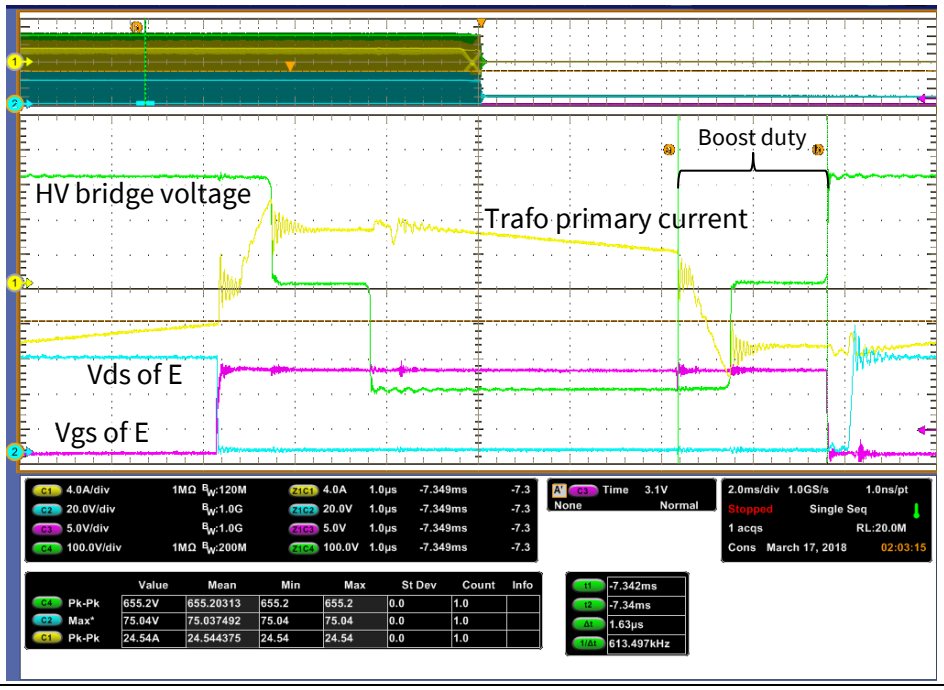

Figure 35 Boost mode duty cycle. Transformer primary current (yellow), LV MOSFET drain voltage (blue), LV MOSFET gate voltage (pink), bridge voltage (green). Note: capture taken at scaled-down voltages.

3.2 Performance and steady-state waveforms

3.2.1 HV full-bridge

The 3300 W bi-directional PSFB ensures full or partial ZVS of the HV MOSFETs at any condition. At light or no load the converter ensures partial ZVS with forced CCM in the LV MOSFETs side and recirculates enough energy for the transitions of the HV bridge (Figure 36).

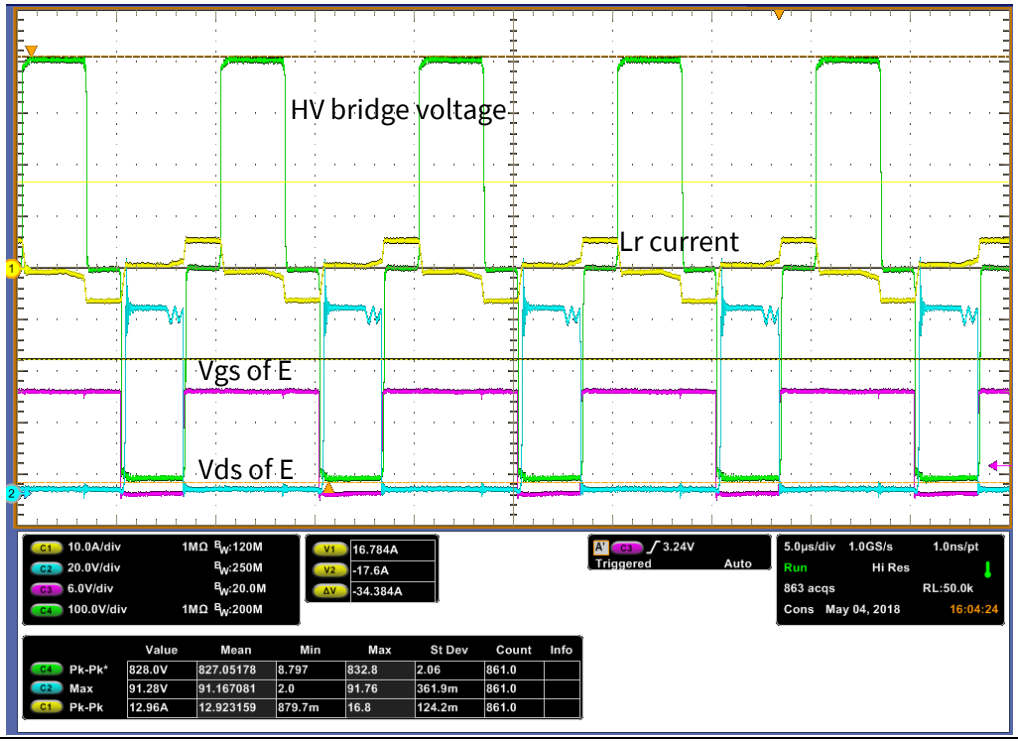

Figure 36 **Partial ZVS of bridge MOSFETs at no load. Resonant inductance current (yellow), LV MOSFET drain voltage (blue), LV MOSFET gate voltage (pink), bridge voltage (green).**

3.2.2 LV bridge

In boost mode the LV MOSFETs are hard-switched turned on (Figure 37). This is the major contribution to loss difference between buck and boost mode (total E_{OSS} of LV MOSFETs is relatively high) and the major reason for the difference in performance (Figure 2) between modes.

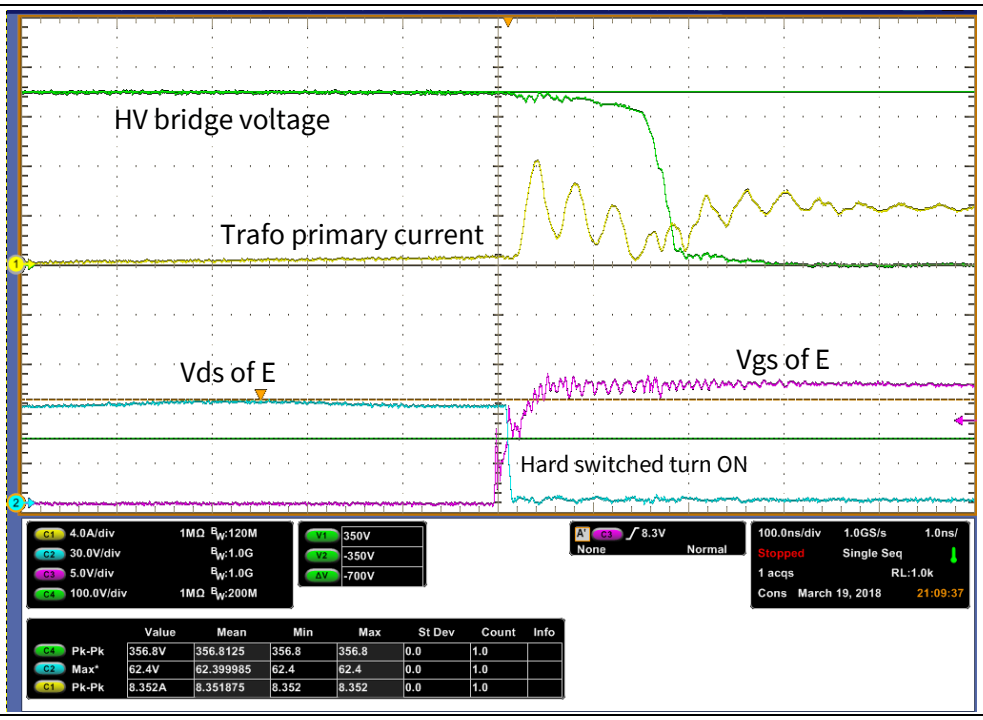

Figure 37 **Hard-switched turn-on of LV MOSFETs**

Drain voltage overshoot of LV MOSFETs, like in buck mode, is well within the derated maximum (120 V), e.g. around 92 V in Figure 36.

3.2.3 Start-up

The converter requires, in boost mode, that the HV rail is pre-charged to a minimum voltage before being able to start up (see Figure 25).

In a non-isolated boost converter a bypassing diode pre-charges the HV rail. However in an isolated boost converter it would require rather more complex auxiliary circuitry.

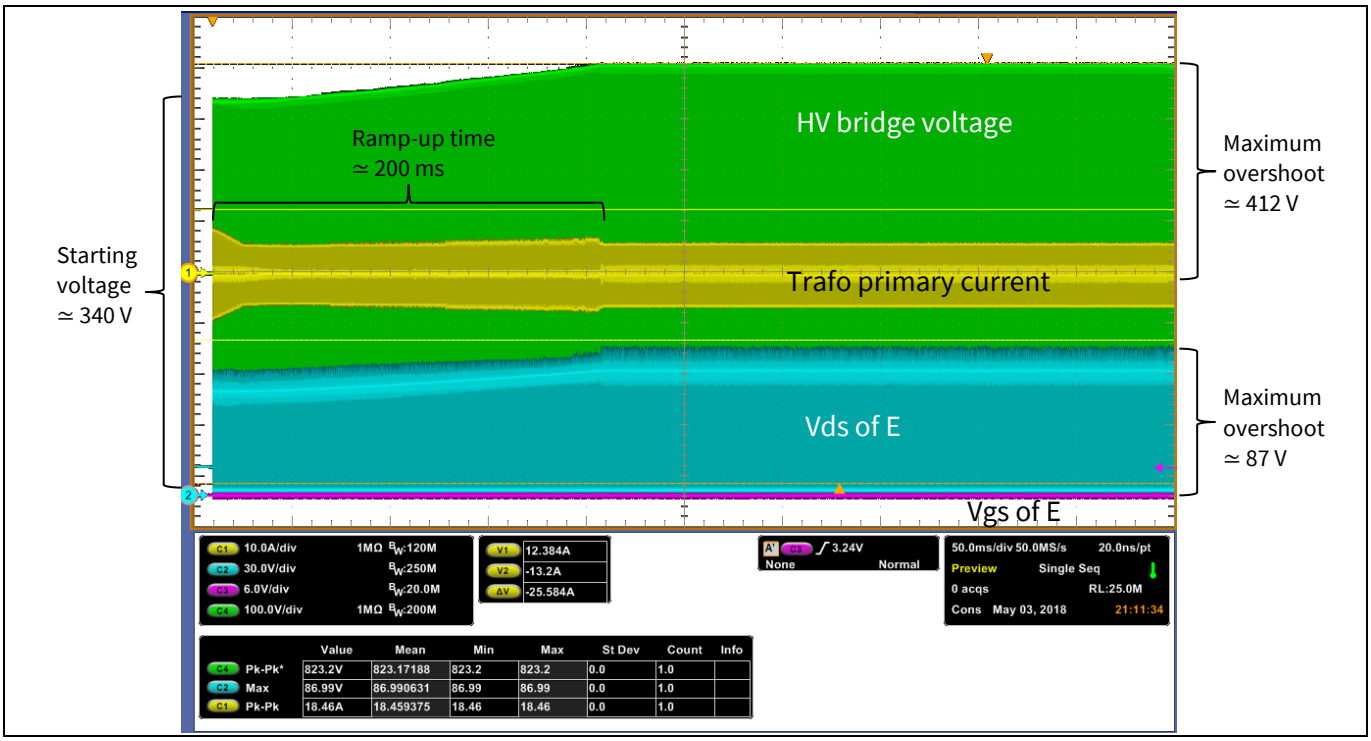

Figure 38 **Soft-start sequence, first pulses ensuring near ZVS for bridge transitions**

The soft-start sequence ensures full or partial ZVS of the HV MOSFETs from the very first pulses, with low- or no-drain voltage overshoot and smooth transitions. The highest drain voltage overshoot is, like in buck mode, at full load due to high-current hard-switched turning off (di/dt induced overshoot by parasitic inductances) (Figure 38 and Figure 39).

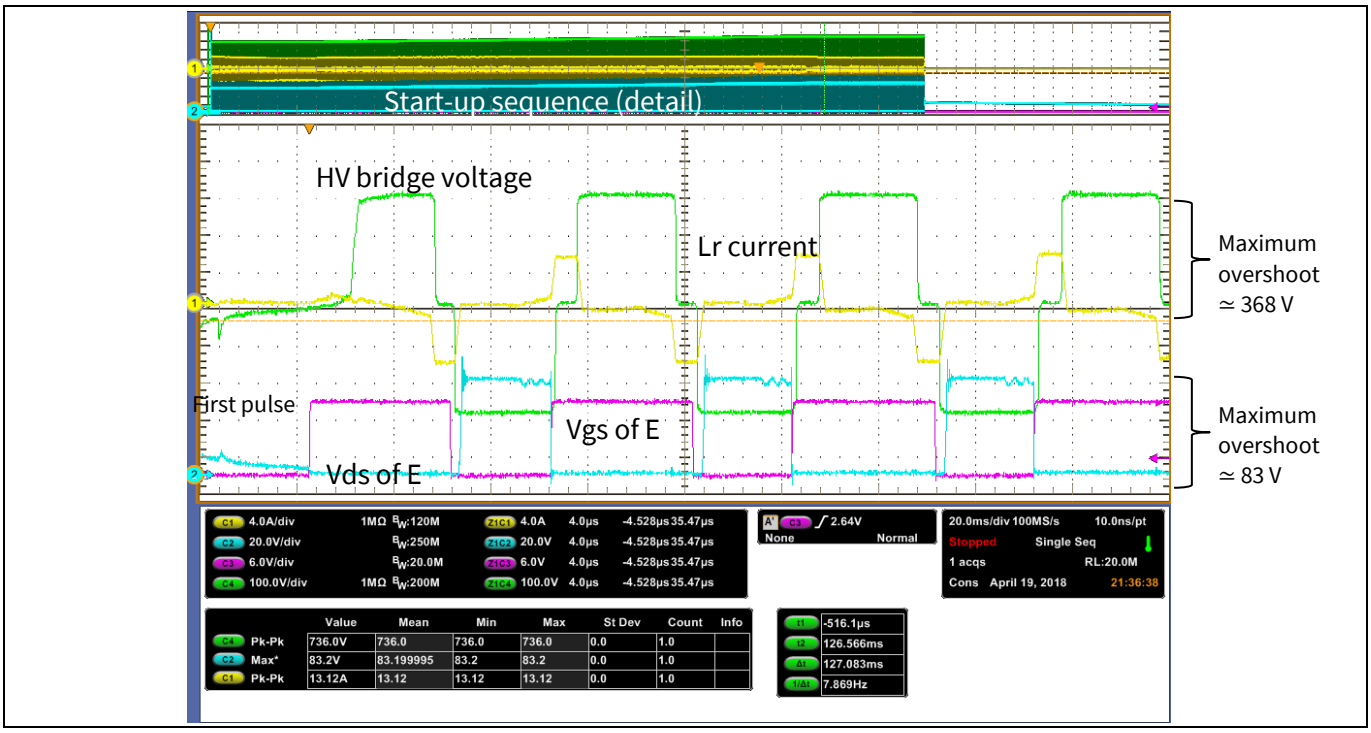

Figure 39 **Soft-start sequence, first pulses ensuring near ZVS for bridge transitions. Note: scaled voltages test capture.**

3.2.4 Burst mode

In boost mode the converter remains switching and recirculating enough energy for partial ZVS of the HV MOSFETs at light or no load. Burst would be visible if the output voltage rises above nominal regulation level (i.e. load jump) (Figure 40).

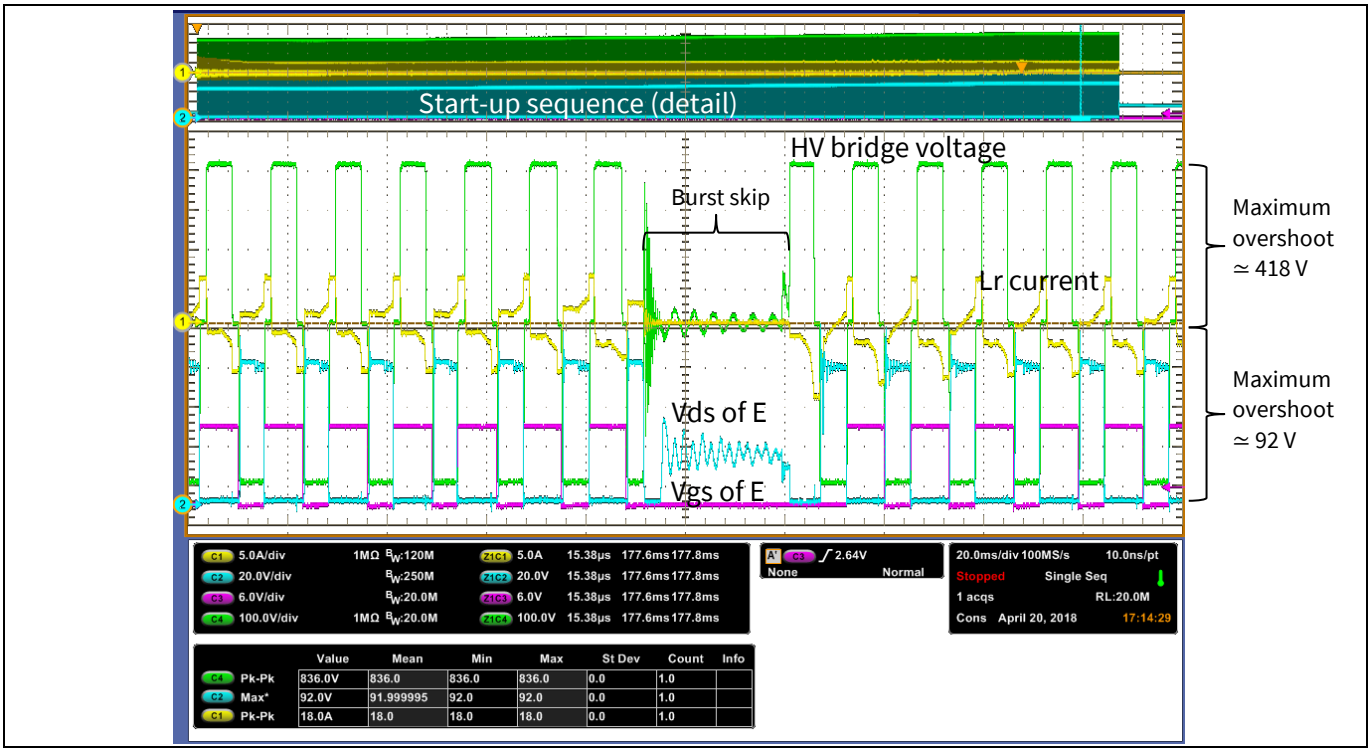

Figure 40 **Burst sequence**

3.3 Thermal map

The losses distribution has similar values in boost and in buck mode operation of the converter, with the main difference being the hard-switching turning-on of the LV MOSFETs (Figure 37) and the conduction time of the clamping diodes.

At no load, unlike the control applied in buck mode, the converter does not stop switching but recirculates energy for near-ZVS transitions of the HV bridge.

Figure 41 shows the temperature rise on the HV bridge due to partial hard-switching (fan speed is at minimum in this condition, contributing to the temperature increase), but still only 33°C (25°C ambient).

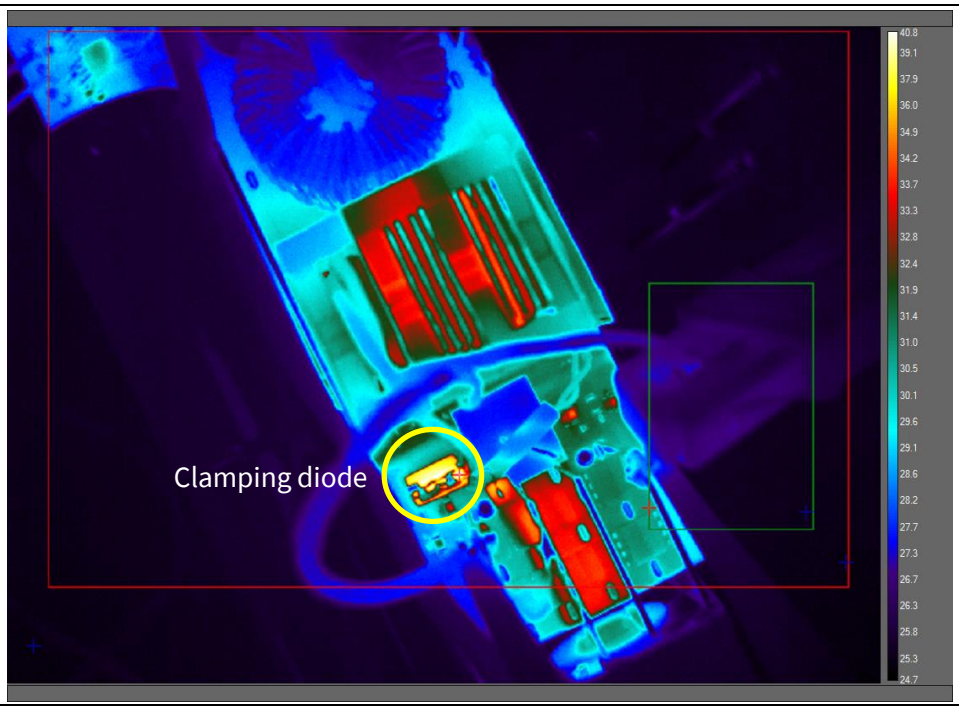

Figure 41 **Thermal capture at no load. In boost mode converter does not stop switching, recirculates current enough for partial bridge ZVS. Front view.**

At full load the main difference with the buck mode capture is the temperature on the clamping diodes and the LV MOSFETs (hard-switched turned on in this mode).

The clamping diodes' average conducted current is higher than in buck mode, also one major contribution to the difference in performance between buck and boost mode (Figure 2).

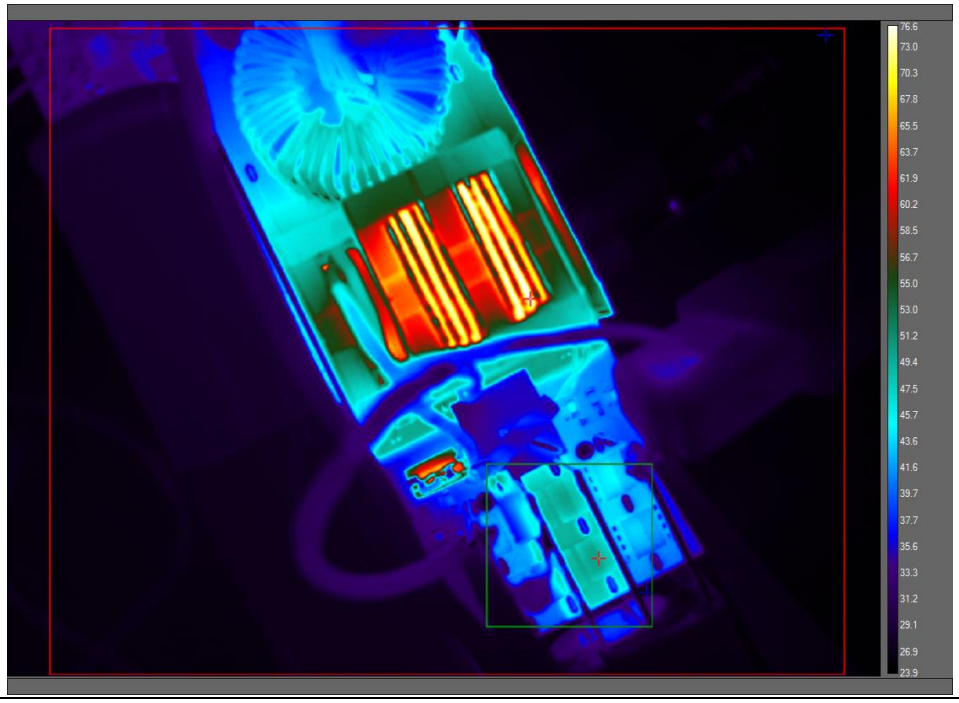

Figure 42 **Thermal capture at full load – front view**

4 User interface

The controller includes serial communication interface (UART) and protocol allowing the parametrization of HV and LV MOSFET timings, output voltage setting, protections activation/deactivation and monitoring of status.

The user interface for windows (Figure 43) is an example of the capabilities of the included communication library within the controller. The user interface was developed to communicate with the controller through **XMC™ Link** (converts UART to USB).

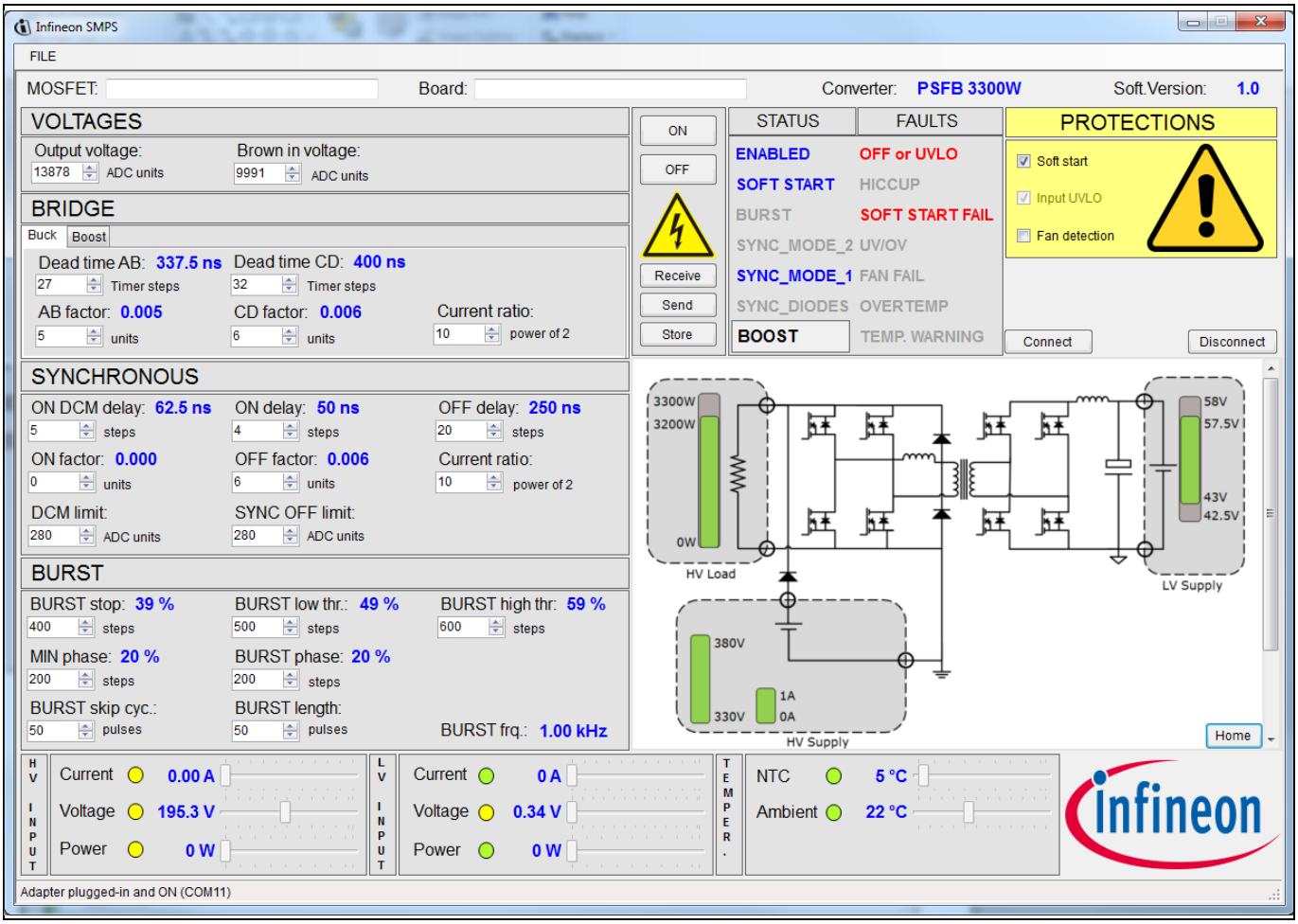

Figure 43 **3300 W bi-directional PSFB advanced user interface**

There are two available versions of the GUI:

- Advanced user interface with run-time parametrization capabilities of dead-times, voltage and current thresholds, protections and working modes
- Simplified user interface intended for monitorization of converter during run-time (Figure 44)

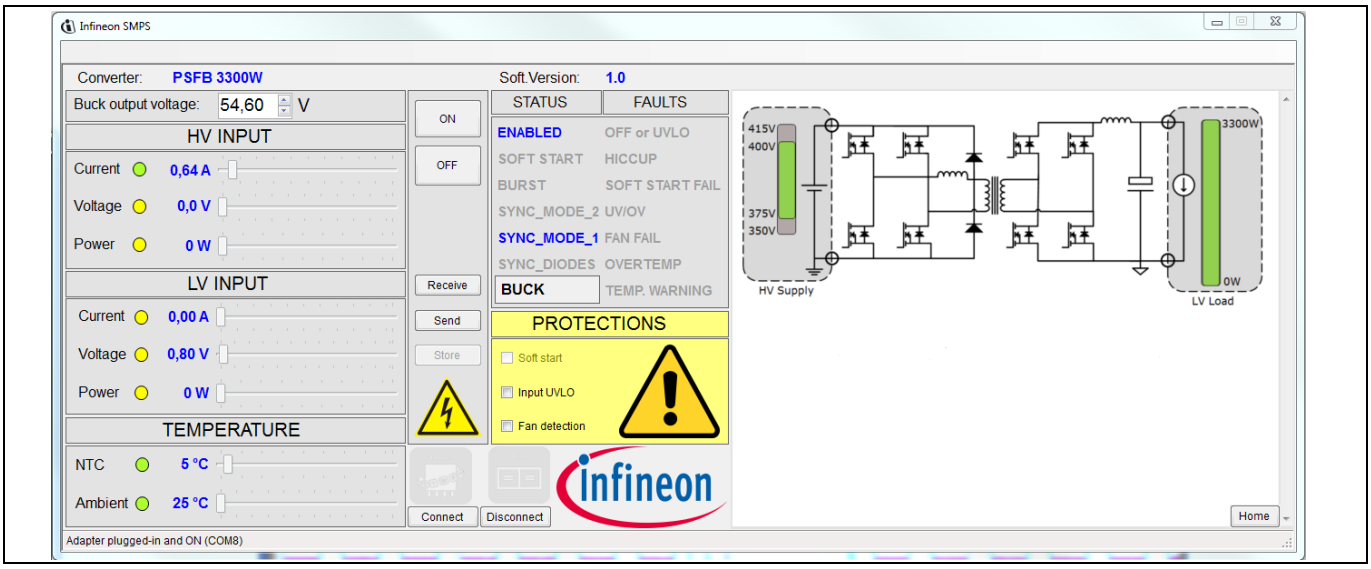

Figure 44 **3300 W bi-directional PSFB simplified user interface**

5 Summary

This document introduces a complete Infineon system solution for a 3300 W bi-directional DC-DC converter which achieves 98 percent efficiency in buck mode and 97 percent in boost mode. The achieved power density is in the range of 4.34 W/cm^3 (71.19 W/in^3), which is enabled by the use of SMD packages and the innovative stacked magnetic construction.

Infineon CoolMOS™ CFD7 in ThinPAK package, the latest and best-performing fast body diode device from Infineon combined with a low parasitic package and an optimized layout achieves great performance with minimum stress, also enabled by the innovative cooling concept presented in this board.

This DC-DC converter proves the feasibility of PSFB topology as high-efficiency topology at the level of fully resonant topologies when combined with the latest Infineon technologies.

This DC-DC converter also proves that PSFB topology can be used as a bi-directional DC-DC stage without changes in the standard design or construction of a traditional and well-known topology by innovations in control techniques powered by digital control and XMC™ Infineon microcontrollers.

6 Schematics

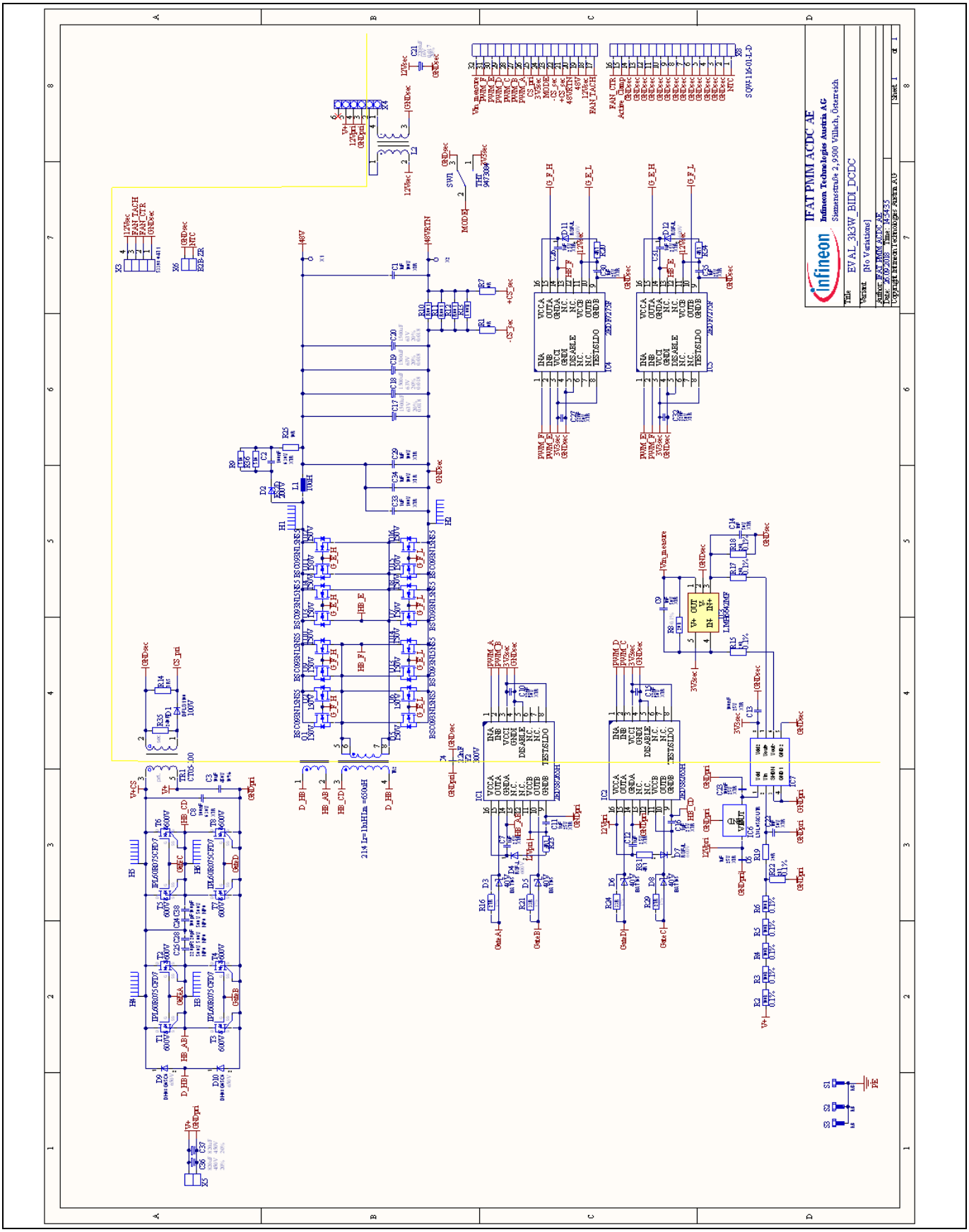

Figure 45 3300 W bi-directional PSFB main board with IPL60R075CFD7 and BSC093N15NS5

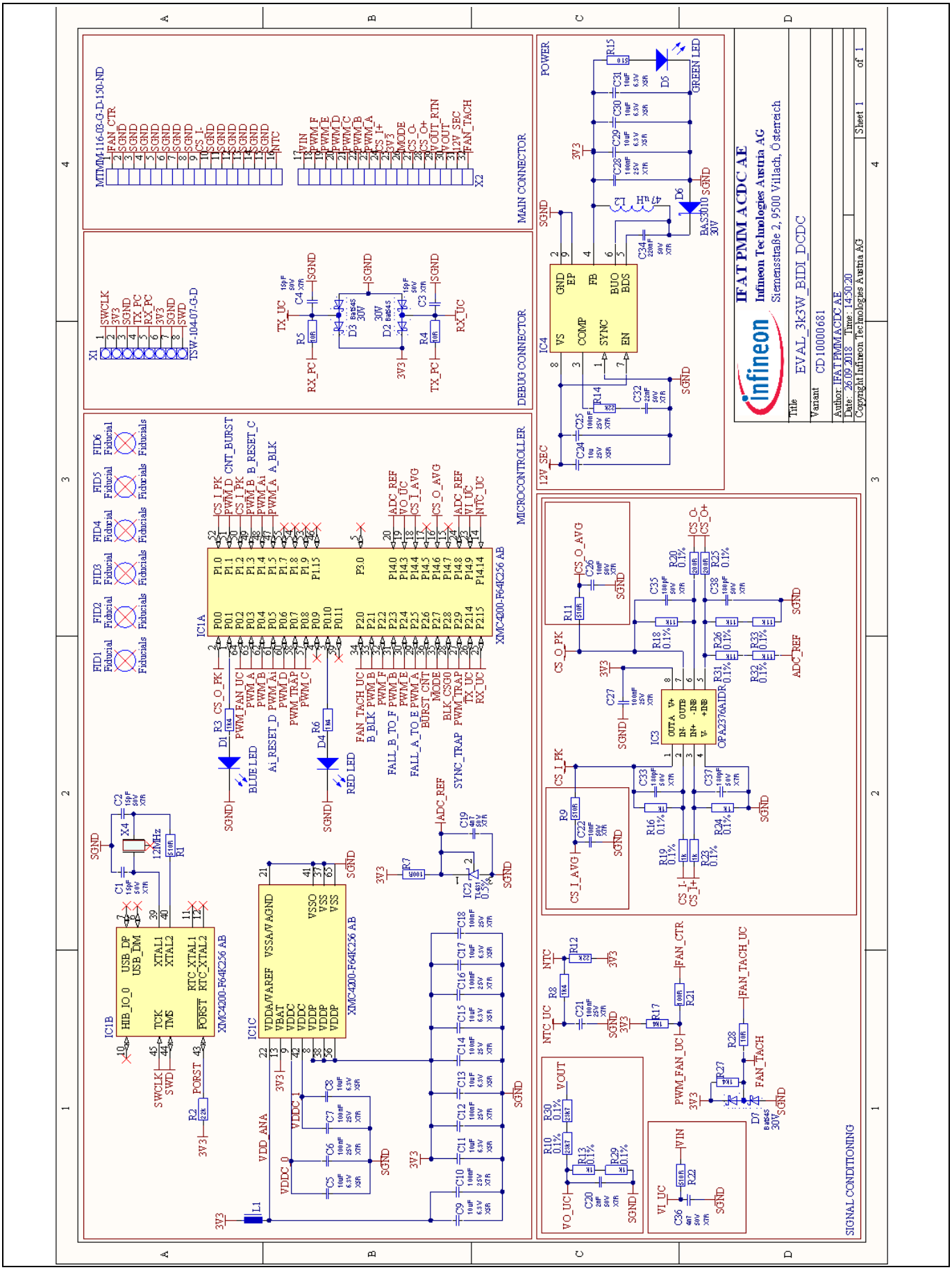

Figure 46 **3300 W bi-directional PSFB controller card with XMC4200-F64K256AB**

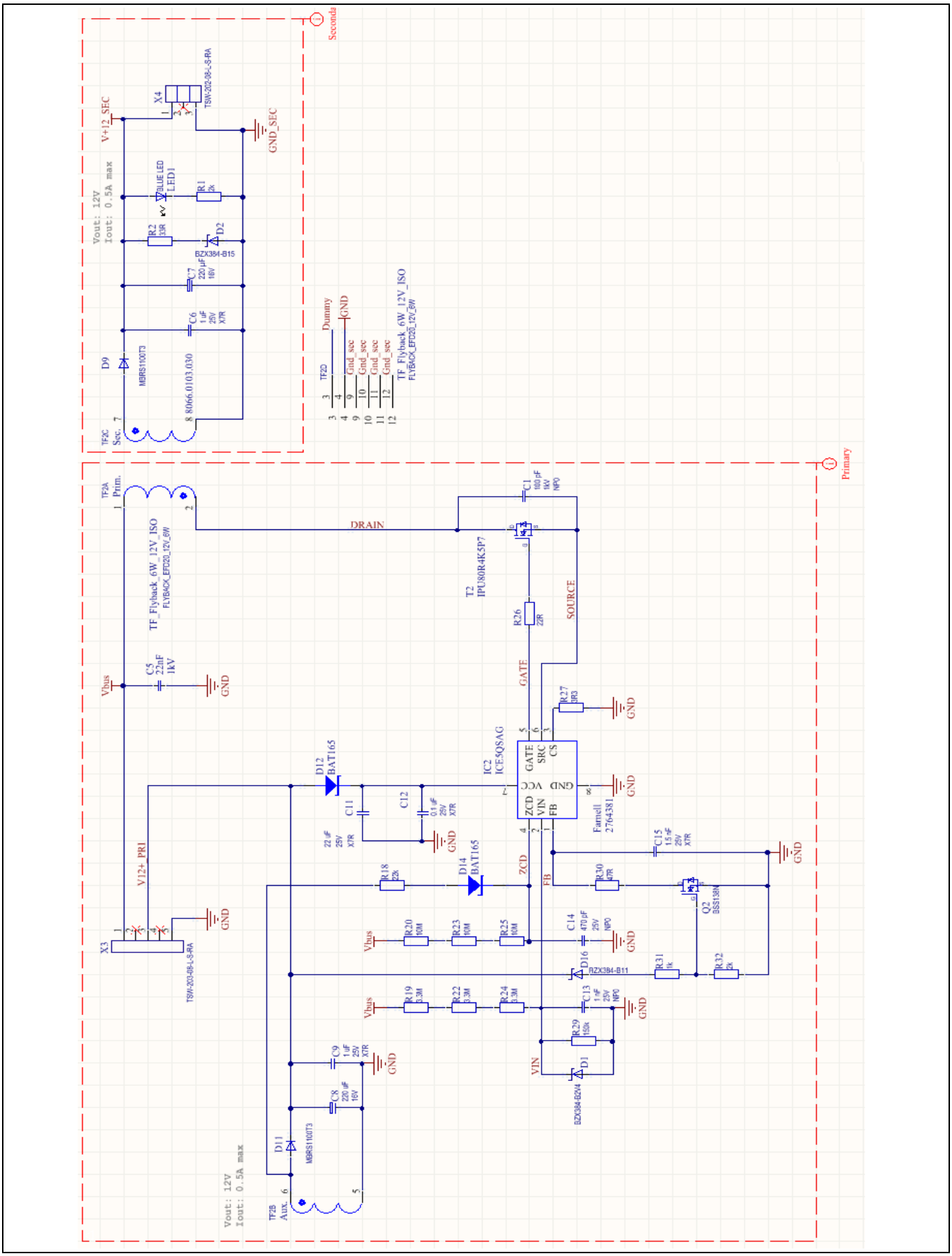

Figure 47 **Auxiliary 6 W power supply**

7 Bill of Materials (BOM)

Parts designators in bold are produced by Infineon.

Table 2 Main board components

Designator	Value	Tolerance	Voltage	Description	Comment
T1, T2, T3, T4, T5, T6, T7, T8	**IPL60R075CFD7**		**600 V**	**nMOSFET**	**SMD**
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16	**BSC093N15NS5**		**150 V**	**nMOSFET**	**SMD**
IC1, IC2	**2EDS8265H**			**Driver IC**	**SMD**
IC4, IC5	**2EDF7275F**			**Driver IC**	**SMD**
D9, D10	**IDH08G65C6**		**650 V**	**Schottky diode**	**THT**
D3, D5, D6, D8	**BAT165**		**40 V**	**Schottky diode**	**SMD**
C1, C5, C29, C33, C34	1 µF	X7R	100 V	Ceramic capacitor	SMD
C2, C8	100 nF	X7R	630 V	Ceramic capacitor	SMD
C3	10 µF	10 percent	450 V	Foil capacitor	THT
C4	4.7 nF	Y2	300 V	Ceramic capacitor	THT
C6, C7, C11, C12, C16, C26, C30, C31, C35	1 µF	X7R	25 V	Ceramic capacitor	SMD
C9, C14	1 nF	X7R	50 V	Ceramic capacitor	SMD
C10, C15, C27, C32	22 nF	X7R	50 V	Ceramic capacitor	SMD
C13, C23	100 nF	X7R	25 V	Ceramic capacitor	SMD
C17, C18, C19, C20	1500 µF	20 percent	63 V	Electrolytic capacitor.	THT
C21	2200 µF	20 percent	16 V	Electrolytic capacitor	THT
C22	10 nF	X7R	25 V	Ceramic capacitor	SMD
C25, C28	220 pF	NP0	500 V	Ceramic capacitor	SMD
C36, C37	820 µF	20 percent	450V	Polarized capacitor	THT
D1	DFLS1100		100 V	Standard diode	SMD
D2	ES2D		200 V	Standard diode	SMD
D4, D7, D11, D12	RSFJL		600 V	Diode	SMD
D13	SMBJ85			Zener diode	SMD
IC3	LMH6642MF			Integrated circuit	SMD
IC6	L78L05ACUTR			Integrated circuit	SMD
IC7	ACPL-C87BT			Optocoupler	SMD
L1	6 µH			Inductor	THT
R1, R7	0 R	1 percent		Resistor	SMD
R2, R3, R4, R5, R6	100 k	0.1 percent		Resistor	SMD

Designator	Value	Tolerance	Voltage	Description	Comment
R8, R15, R17, R18	20 k	0.1 percent		Resistor	SMD
R10, R11, R12, R13	R001	1 percent		Resistor	SMD
R14, R25	10 R	1 percent		Resistor	SMD
R16, R29	27 R	1 percent		Resistor	SMD
R19	39 R	1 percent		Resistor	SMD
R20, R23, R31, R34	4R7	1 percent		Resistor	SMD
R21, R24	33 R	1 percent		Resistor	SMD
R22	2 k	0.1 percent		Resistor	SMD
R26, R35	1K2	1 percent		Resistor	SMD
R36	1 k	1 percent		Resistor	SMD
TR1	CT05-100			Transformer	THT
TR2				Transformer	THT
X1, X2	P2A-PCB-SS			Connector	THT
X3	53398-0471			Connector	SMD
X5	Two-pole connector			Connector	THT
X6	B2B-ZR			Connector	THT
X8	SQW-116-01-L-D			Pin header 2 x 16 contacts	THT

Table 3 Control board components

Designator	Value	Tolerance	Voltage	Description	Comment
IC1	**XMC4200-F64K256 AB**			**Integrated circuit**	**SMD**
IC4	**IFX91041EJ V33**			**IC buck**	**SMD**
C1, C2, C3, C4	15 pF	X7R	50 V	Ceramic capacitor	SMD
C5, C8, C9, C11, C13, C15, C17, C29, C30, C31	10 µF	X5R	6.3 V	Ceramic capacitor	SMD
C6, C7, C10, C12, C14, C16, C18, C21, C25, C27, C28	100 nF	X7R	25 V	Ceramic capacitor	SMD
C19, C36	4n7	X7R	50 V	Ceramic capacitor	SMD
C33, C35, C37, C38	180 pF	X7R	50 V	Ceramic capacitor	SMD
C20	2 nF	X7R	50 V	Ceramic capacitor	SMD
C22, C26	10 nF	X7R	50 V	Ceramic capacitor	SMD
C24	10 µF	X5R	25 V	Ceramic capacitor	SMD
C32	22 nF	X7R	50 V	Ceramic capacitor	SMD
C34	220 nF	X7R	50 V	Ceramic capacitor	SMD
D1	Blue LED			LED	SMD
D2, D3, D7	Bat54S		30 V	Schottky diode	SMD

Designator	Value	Tolerance	Voltage	Description	Comment
D4	Red LED			LED	SMD
D5	Green LED			LED	SMD
D6	BAS3010		30 V	Schottky diode	SMD
IC2	TL431	0.5 percent		Integrated circuit	SMD
IC3	OPA2376AIDR			Integrated circuit	SMD
L1	Ferrite bead 60 Ω at 100 MHz			Inductor	SMD
L2	47 µH			Inductor	SMD
R1, R9, R11, R22	510 R	1 percent		Resistor	SMD
R2, R12, R14	22 k	1 percent		Resistor	SMD
R3, R6, R8, R17, R27	1k4	1 percent		Resistor	SMD
R4, R5, R28	10 R	1 percent		Resistor	SMD
R7, R21	100 R	1 percent		Resistor	SMD
R10, R30	23k7	0.1 percent		Resistor	SMD
R18, R26, R31, R32, R33	11 k	0.1 percent		Resistor	SMD
R13, R16, R19, R23, R24, R29	1 k	0.1 percent		Resistor	SMD
R15	510	1 percent		Resistor	R15
R20, R25	200 R	0.1 percent		Resistor	R20, R25
X1	TSW-104-07-G-D			Female header 8 contacts	THT
X2	TMM-116-03-L-D			Pin header 2 x 16 contacts	THT
X4	12 MHz			Crystal oscillator	SMD

8 References

[1] "800 W ZVS phase-shift full-bridge evaluation board. Using 600 V CoolMOS™ CFD7 and digital control by XMC4200", AN_201709_PL52_027

[2] "1400 W ZVS phase-shift full-bridge evaluation board. Using 600 V CoolMOS™ CFD7 and digital control by XMC4200", AN_201711_PL52_003

[3] Jared Huntington, "6 W bias supply. Using the new 800 V CoolMOS™ P7, ICE5QSAG QR flyback controller, and snubberless flyback for improved auxiliary power-supply efficiency and form factor", AN_201709_PL52_030

[4] F. Krismer, J. Biela, J. W. Kolar, "A Comparative Evaluation of Isolated Bi-directional DC-DC Converters with Wide Input and Output Voltage Range", in Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005

[5] A. Hillers, D. Christen and J. Biela, "Design of a Highly Efficient Bi-directional Isolated LLC Resonant Converter", in Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International

Revision history

Major changes since the last revision

Page or reference	Description of change

Other Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2018-05-02

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2019 Infineon Technologies AG.
All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN_1809_PL52_1809_081412

IMPORTANT NOTICE
The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.