2.7 kW Titanium server digital power supply with CoolSiC™ 650 V and XMC™ MCUs

About this document

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Scope and purpose

This application note describes a high-density and high-efficiency PSU targeted towards enterprise server applications and covers the design and implementation of a 2.7 kW dual-stage AC-DC power supply utilizing highly efficient CoolSiC™ devices. The power stages are digitally controlled by XMC™ microcontrollers which provide responsive fault protection and stable output regulation.

Additionally, it describes the system in detail, along with critical design guidelines and a control strategy. It also includes setup and testing instructions to help user experience the full benefits of the Infineon products used in the design.

Intended audience

This application note is intended for power electronics engineers who want to verify the performance of the following Infineon products in a server power supply application consisting of bridgeless totem-pole power factor correction (PFC) and LLC topologies:

- CoolSiC™ 650 V, 72 mΩ in bridgeless totem-pole PFC topology
- CoolMOS™ 600 V, 40 mΩ C7 in bridgeless totem-pole PFC topology
- CoolMOS™ 600 V, 24 mΩ CFD7 in LLC topology
- OptiMOS™ 6 MOSFET technology in LLC synchronous rectification
- Digital control with the XMC™ family of microcontrollers
- Isolated and non-isolated gate drivers from the EiceDRIVER™ family
- A digital isolator from the ISOFACE™ product family

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1 Introduction

As the computing power requirements increase, there is a need for higher power availability in the same volume for datacenter server applications.

Figure 1 shows the high-density 2.7 kW 80 PLUS™ Titanium server power supply board. Server PSUs are typically two-stage systems consisting of a front-end AC-DC PFC rectifier that draws high-quality power from the grid and provides a constant DC bus for the subsequent DC-DC stage, as shown in Figure 2. The isolated DC-DC stage is implemented with a highly efficient LLC topology, which provides the regulated bus voltage to the downstream server loads. Utilizing the best-in-class Infineon power devices, gate drivers, and microcontrollers, this system meets and exceeds the stringent 80 PLUS™ Titanium efficiency and power quality requirements.

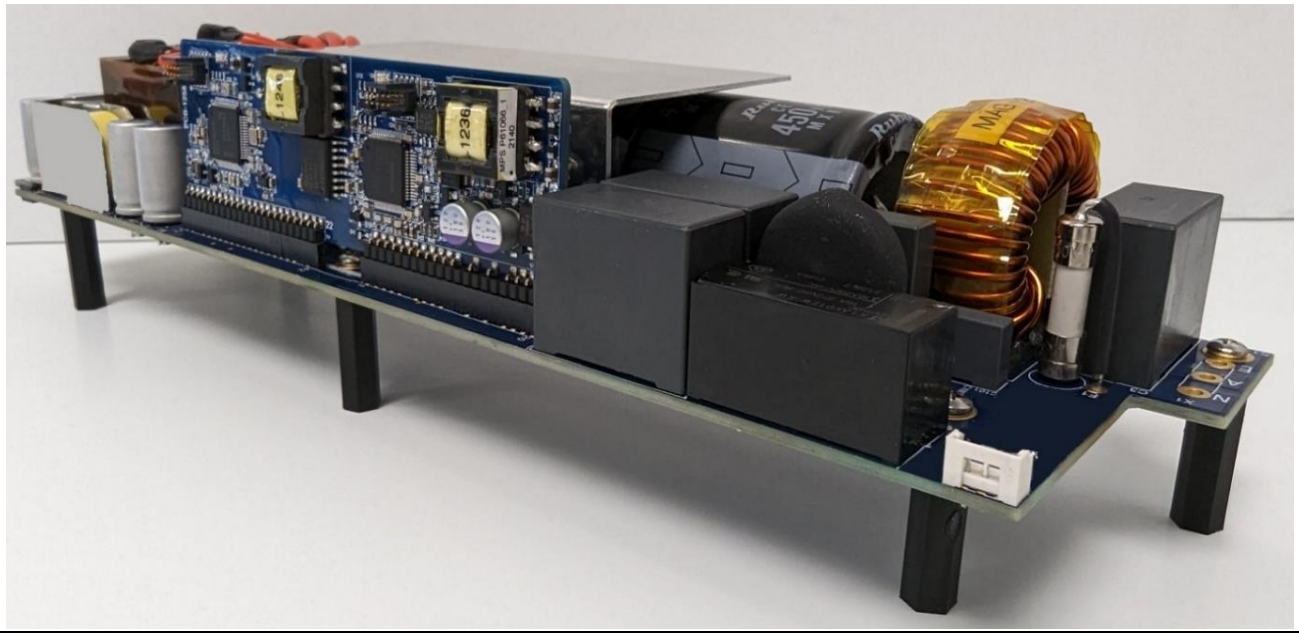

Figure 1 2.7 kW 80 PLUS™ Titanium server power supply board

Introduction

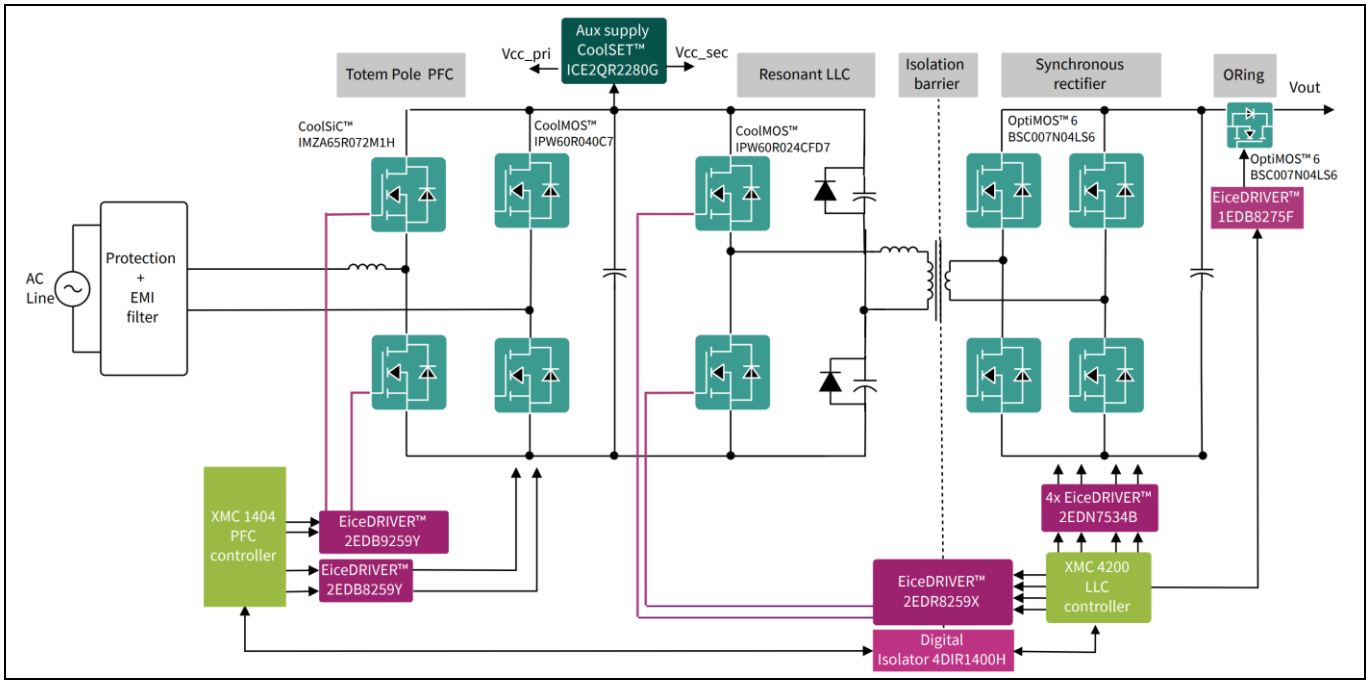

Figure 2 **Typical PSU system block diagram**

1.1 System specifications

This reference design has been developed to meet the following requirements:

Table 1 **Input requirements**

Parameter	Value
Input voltage range	180–264 Vac (2700 W), 90–140 Vac (1500 W)
Frequency	47 Hz to 63 Hz
Efficiency	96% peak, 80 PLUS™ Titanium
Max input current	13.8 Arms at 120/208 Vac
Inrush current	<30 Apk
Surge withstand	>1 kV L-L, >2 kV L-E (EN 61000-4-5)
Power factor	>0.9 beginning at 20% load
ITHD, Harmonics	<10%, EN 61000-3-2
Hold-up time	>10 ms at 100% load
Operating temperature	0 to 50°C

Table 2 **Output requirements**

Parameter	Value
Nominal output voltage	12.2 V
Total output regulation range	11.2 V to 13.2 V
Output ripple	<180 mVp-p
Output current	224/112 A at the high/low line

Introduction

Parameter	Value
Capacitive loading	4,000 µF to 38,000 µF
Start-up from AC to output	<2 s
Output rise time	<100 ms
Operating temperature	0 to 50°C

Table 3 80 PLUS™ Titanium efficiency requirements*

Percentage of rated load	10%	20%	50%	100%
80 PLUS™ Titanium	90%	94%	96%	94%

* Measured at Vin = 230 Vac, including bias and fan power.

2 Hardware overview

2.1 Power supply board description

The various functional blocks of the PSU are:

- Input stage, which contains the EMI filter, inrush current limiting, and protection components
- Totem-pole boost power factor correction AC-DC stage
- LLC DC-DC conversion stage

Figure 3 and Figure 4 show the top and bottom views of the 2.7 kW PSU with a power density of 54 W/in^3.

Additionally, Figure 5 and Figure 6 show the control and bias boards, which contain the MCU to control the PFC and LLC stages, and the bias power supply, which provides housekeeping power for the PSU.

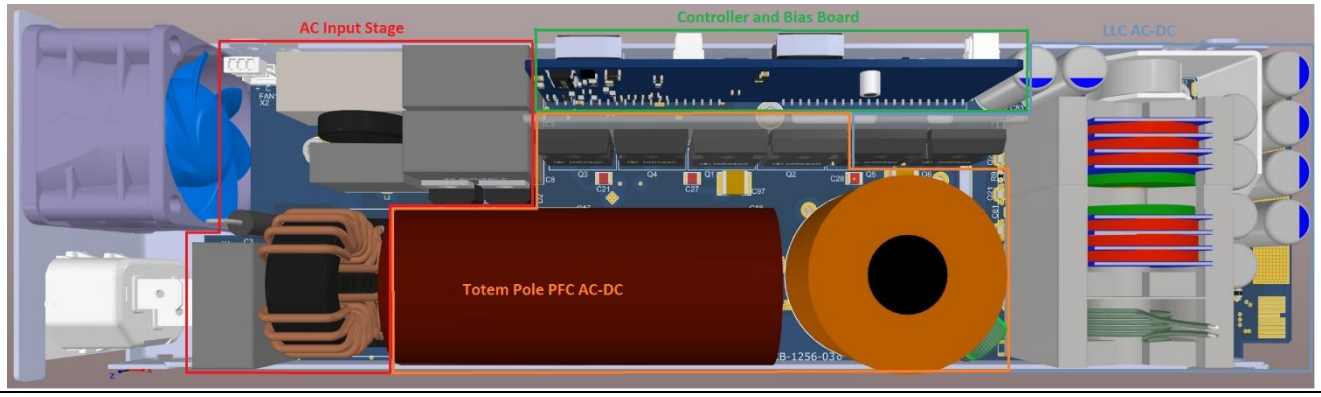

Figure 3 Functional blocks on the PSU board - top view

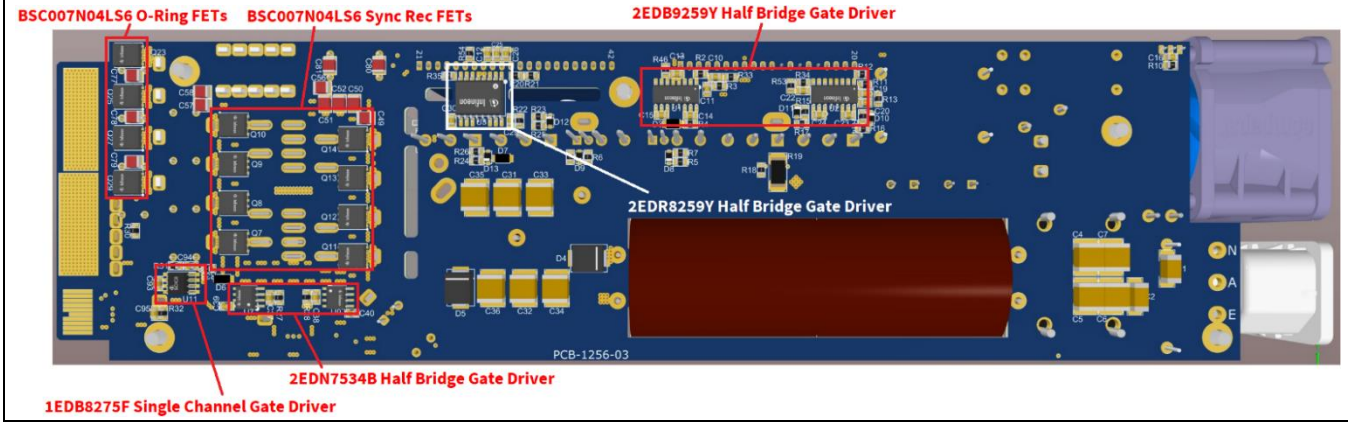

Figure 4 Critical components on the PSU board - bottom view

Hardware overview

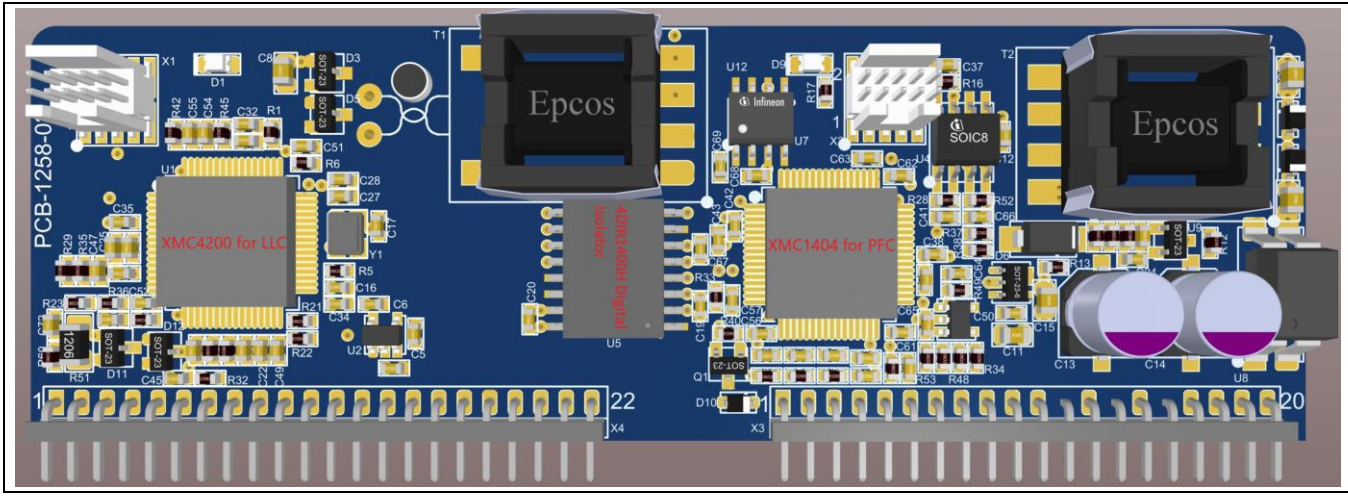

Figure 5 **Controller and bias board – top view**

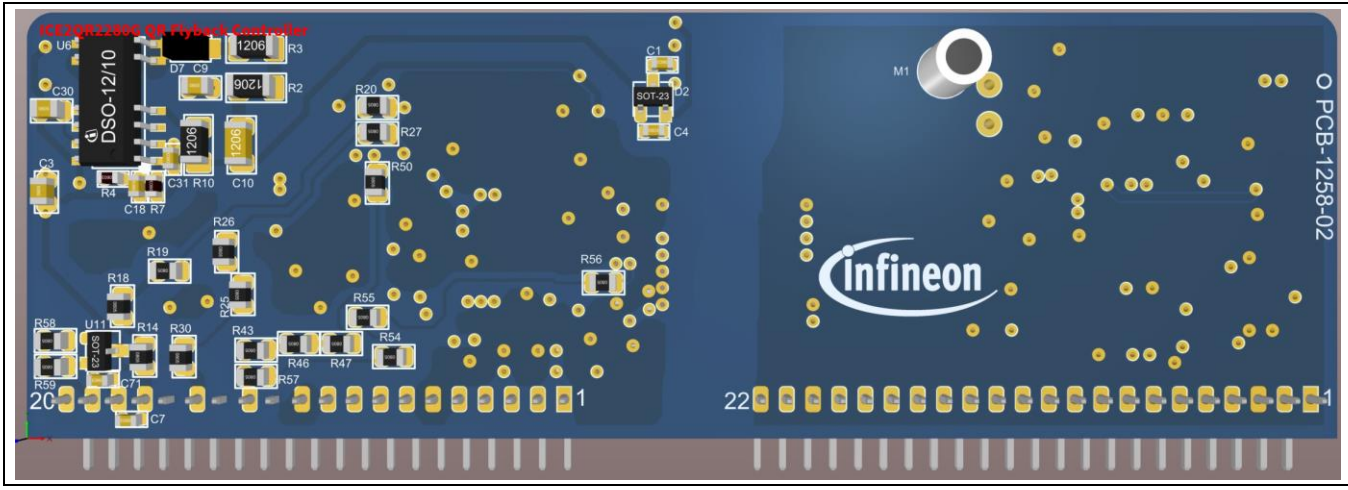

Figure 6 **Controller and bias board – bottom view**

2.2 Infineon products

2.2.1 CoolSiC™ MOSFETs

The AC-DC rectification with power factor correction is achieved by the implementation of a bridgeless totem-pole PFC boost converter operating in a continuous conduction mode (CCM). The hard switching nature of a CCM converter necessitates the use of switching devices with low parasitic capacitances and reverse recovery losses. Infineon's CoolSiC™ 650 V MOSFET meets these requirements and enables the front-end AC-DC rectifier to operate at high efficiencies and quality of power drawn from the grid.

This design uses CoolSiC™ IMZA65R072M1H 650 V MOSFET in a TO247 4-pin package. The 4-pin package reduces parasitic source inductance effects during driving of the device and enables fast switching with high efficiencies. The excellent thermal behavior of CoolSiC™ and the low $R_{DS(on)}$ shift over temperature enable the use of a higher $R_{DS(on)}$ device, which typically has lower capacitances. This leads to lower switching losses, thereby ensuring high operating efficiency. A robust fast body diode with a low reverse recovery charge is critical in a hard-switching topology, both in terms of reliability and efficiency. Its superior gate oxide reliability

combined with the ease of driving enables the use of standard gate drivers, such as the latest generation of isolated gate drivers from the EiceDRIVER™ family.

2.2.2 CoolMOS™ MOSFETs

The AC rectification leg of the bridgeless totem-pole PFC converter uses CoolMOS™ IPW60R040C7 600 V MOSFET. Because these switches operate at a slower rate of AC line frequency, it is critical to minimize the conduction losses. IPW60R040C7 features the best $R_{DS(on)}$*A figure of merit and significantly minimizes the AC line current conduction losses to enable high efficiency across the load range.

Additionally, the primary side of the DC-DC LLC converter uses CoolMOS™ IPW60R024CFD7 600 V MOSFET, an ideal fit for high-frequency resonant topologies such as the LLC converter because of its best-in-class reverse recovery charge, lowest E_{oss}, and $R_{DS(on)}$ x Q_g figure of merit. This device features excellent hard commutation ruggedness in the hard switching regions of LLC operation.

2.2.3 OptiMOS™ MOSFETs

The LLC synchronous rectification is performed using OptiMOS™6 BSC007N04LS6 40 V and 0.7 mΩ MOSFETs. Using MOSFETs for synchronous rectification as opposed to diodes minimizes conduction losses to achieve a high-efficiency and high-power-density power supply. OptiMOS™6 MOSFETs are optimized for low-voltage, high-current synchronous rectification applications. They have a very low $R_{DS(on)}$ that minimizes conduction losses. Their low thermal resistance from junction to bottom makes thermal management easy at full loads. They are rated up to 175°C, which helps designers use fewer devices in parallel to spread out losses and heat. The small footprint of the surface mount package further helps in increasing the system power density.

2.2.4 XMC™ microcontroller

A 32-bit XMC1404 microcontroller digitally controls the bridgeless totem-pole PFC boost converter. XMC1404 is based on an Arm® Cortex®-M0 processor core and is an ideal MCU to address the real-time control needs of a bridgeless TPPFC topology. It contains a fast 12-bit ADC with two sample and hold stages and a 0–5.5 V input range to enable high-resolution sensing for real-time control of the converter. The high-resolution ADC, in conjunction with a 16-bit 96 MHz Capture/Compare Unit 8 (CCU8) timer for PWM, ensures that the PFC controller achieves the goals of high power quality, tight output regulation, and good dynamic line and load response.

The second-stage LLC DC-DC converter is implemented and controlled using the powerful XMC4200 MCU, which is based on Arm® Cortex®-M4 with a built-in DSP instruction set. It comes with a comprehensive set of fast and precise analog/mixed signal, timer/PWM, and communication peripherals. The following are the features of XMC4200 that make it well suited to implement a resonant topology like LLC, which depends on fine adjustment of switching dead times:

- Up to 4x 12-bit ADC with a sample time of 70 ns ensures fast reaction times and tighter control loops
- 4-channel, 150 ps HRPWM timer
- One CCU8 for motor control and power conversion
- High-performance 32-bit Arm® Cortex®-M4 CPU

2.2.5 EiceDRIVER™ gate drivers

The following gate drivers from the EiceDRIVER™ family are used in this design:

- 2EDB9259Y is used on the PFC fast legs. This is a dual-channel isolated gate driver IC with floating outputs. The strong 5 A/9 A source/sink dual-channel gate driver comes with a very high 150 V/ns common-mode transient immunity (CMTI) for robust operation with CoolSiC™ MOSFETs in a high-power switching noise environment.
- 2EDB8259Y is used on the PFC slow legs for driving the CoolMOS™ MOSFETs. This part is similar to 2EDB9259Y, but with a lower UVLO of 8 V to be compatible with the driving levels of CoolMOS™ MOSFET.
- 2EDR8259X is used to drive the primary switches in the LLC DC-DC converter. It is a reinforced isolated gate driver IC to drive the LLC primary switches across the isolation boundary because the XMC4200 MCU is located on the low-voltage side. The strong 5 A/9 A source/sink dual-channel gate driver comes with a very high 150 V/ns CMTI for robust operation with CoolMOS™ MOSFETs, CoolGaN™ GIT HEMTs, and a high-power switching noise environment. It features symmetrical operation in a bootstrapped system to reduce the risk of saturation of the main transformer or hard commutation in an LLC.
- 2EDN7534B is used to drive the low-voltage synchronous rectifier of the LLC DC-DC converter. This gate driver comes in a small SOT-23 footprint to increase the power density of the solution. High output current capability, tight timing specifications, and reduced output start-up and shutdown times make the 2EDN family the first choice for many fast-switching applications.

2.2.6 ISOFACE™ digital isolator

In this reference design, the XMC1404 PFC controller is located on the high-voltage side, whereas the LLC controller XMC4200 is located on the 12 V side of the board. The communication between these two controllers must be implemented over the reinforced isolation barrier to satisfy system-level safety requirements. The 4DIR1400H digital isolator is a perfect fit for this use case, with the following features:

- High common-mode transient immunity > 100 kV/µs
- VISO of 5700 V_{rms} (UL1577), VDE 0884-17
- Wide supply voltage range from 2.7 V to 6.5 V (absolute maximum 7.5 V)
- Accurate timing with a 26 ns typical propagation delay and -6/+7 ns spread
- Low power consumption with a maximum 3.3 mA at 3.3 V and 1 Mbps
- The fail-safe default output is low
- Low power consumption

3 Hardware design considerations

3.1 Bridgeless totem-pole PFC

This section describes the design and selection of the critical components of the first-stage bridgeless totem-pole PFC.

Table 4 shows the specifications of the PFC section.

Table 4 PFC specifications

Parameter	Value
Input voltage range	180–264 Vac (2700 W), 90-140 Vac (1500 W)
Output voltage	400 V
Power factor	>0.9 beginning at 20% load
ITHD, Harmonics	<10%, EN 61000-3-2
Hold-up time	>10 ms at 100% load
Switching frequency	65 kHz

As mentioned in [1], there is a relationship between the single-stage PFC switching frequency and the EMI filter cut-off frequency. From Figure 7, you can see that the optimal switching frequency for a single-stage PFC is just below 75 kHz. For this design, 65 kHz is chosen to ensure that the second harmonic is below the measurement start of 150 kHz and minimize hard switching losses.

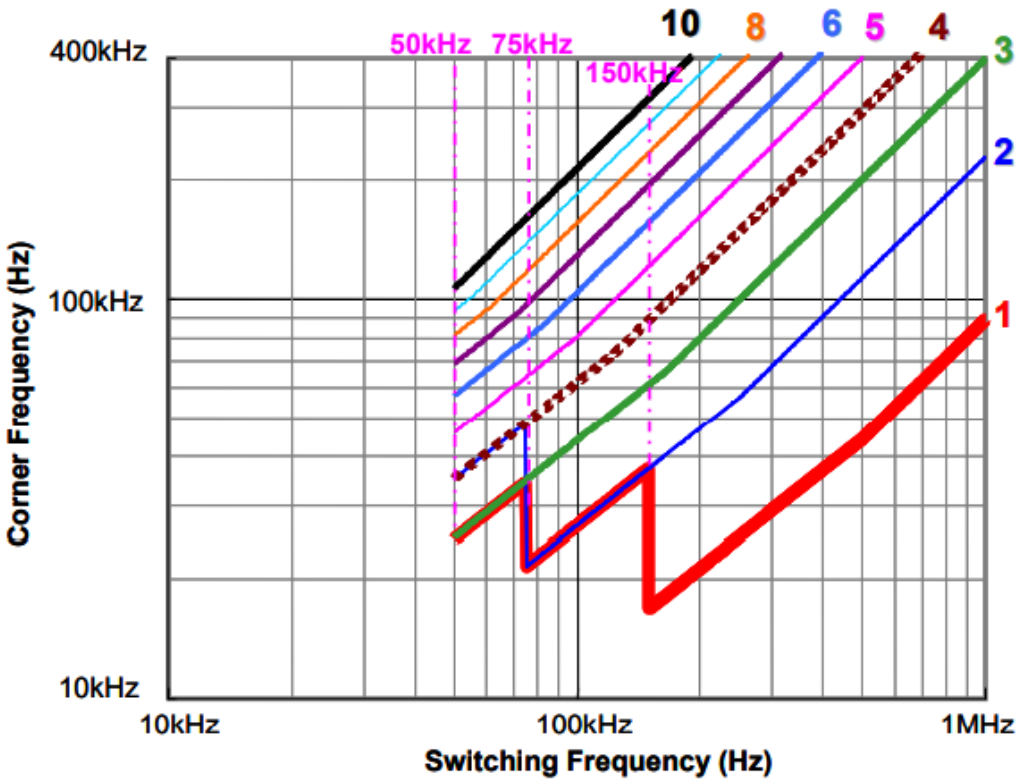

Figure 7 Relationship between switching frequency and EMI filter corner frequency (see [1])

3.1.1 CoolSiC™ MOSFET selection

As mentioned earlier, CoolSiC™ MOSFET is an ideal fit for a hard-switching topology like the bridgeless totem-pole PFC. The main goal of using a CoolSiC™ MOSFET in this design is to minimize both conduction and switching losses to maximize the efficiency and power density. The CoolSiC™ MOSFET has significantly better figures of merit, which helps it outperform silicon superjunction MOSFETs in topologies that have third-quadrant operation.

The parametric advantage of CoolSiC™ MOSFET over silicon SJ MOSFETs is described in detail [2]. This application note also describes the process of selecting the optimum $R_{DS(on)}$ for a design by considering the power level, switching frequency, and load at which peak efficiency or best thermal performance is desired. For this design, a CoolSiC™ IMZA65R072M1H 650 V MOSFET is selected, which has a nominal $R_{DS(on)}$ of 72 mΩ.

After selecting an $R_{DS(on)}$ class, calculate the total losses (conduction plus switching) at the highest loss operating condition to ensure that the losses do not exceed the thermal management capability of the design and satisfy the efficiency criteria.

In the bridgeless totem-pole boost PFC, each CoolSiC™ MOSFET operates as a boost switch during one half of the AC cycle and as a rectifier during the other half. Therefore, according to the following equations, the losses for each half of the AC cycle must be calculated and averaged to find the total loss per device over the full line cycle.

First, define the operating conditions under which the converter needs to be designed and analyzed.

$V_{in_rms} := 230\ V$ — Input RMS voltage

$V_{in_pk} := V_{in_rms} \cdot \sqrt{2} = 325.269\ V$ — Peak of input voltage

$V_{out} := 400\ V$ — PFC output voltage

$F_s := 65\ kHz$ — PFC switching frequency

$P_{oLLC} := 2700\ W$ — Full load output power

$\eta_{LLC} := 96\%$ — Efficiency of LLC stage at full load

$P_{oPFC} := \frac{P_{oLLC}}{\eta_{LLC}} = 2.813\ kW$ — PFC stage output power

$T_s := \frac{1}{F_s} = 15.385\ \mu s$ — Switching period

$DeadTime := 300\ ns$ — PFC fast leg dead time

$V_g := 15\ V$ — CoolSiC™ gate drive voltage

Hardware design considerations

$Q_g := 22\ nC$ CoolSiC™ gate charge

$R_{dson} := 0.072\ \Omega$ CoolSiC™ on state resistance

CoolSiC™ losses as a boost switch

Conduction loss

$$I_Q := \frac{P_{oPFC}}{V_{in_rms}} \cdot \sqrt{1 - \frac{8}{3 \cdot \pi} \cdot \frac{V_{in_pk}}{V_{out}}} = 6.806\ A$$

Boost switch RMS current

$$P_{Q_cond} := I_Q^{\ 2} \cdot R_{dson} \cdot 1.2 = 4.002\ W$$

Conduction loss including $R_{DS(on)}$ temperature coefficient at 125°C

Switching loss

The method of calculating the switching losses is shown in [2] and is used to estimate the switching losses in this design.

$$I_{Lavg} := \frac{P_{oPFC}}{V_{in_rms}} \cdot \frac{2 \cdot \sqrt{2}}{\pi} = 11.009\ A$$

Average inductor current during switching transitions

$$E_{on_off} := \left(\frac{1.85}{1\ A} \cdot I_{Lavg} + \frac{1.24\ \Omega}{R_{dson}} \right) \cdot 10^{-6}\ J = \left(3.759 \cdot 10^{-5}\right)\ J$$

Average of turn on and turn off energy

$$P_{Q_sw} := E_{on_off} \cdot F_s = 2.443\ W$$

Switching loss

$$P_{Q_GD} := V_g \cdot Q_g \cdot F_s = 0.021\ W$$

Gate drive loss

Total loss during switch mode

$$P_{Q_tot} := P_{Q_cond} + P_{Q_sw} + P_{Q_GD} = 6.467\ W$$

CoolSiC™ MOSFET losses as a boost rectifier

During the other AC half cycle, the same CoolSiC™ MOSFET that acts as the switch during the previous half cycle now operates as a synchronous boost rectifier. Initially, the current flows through the body diode during the dead time, resulting in body diode VI loss. At high switching frequencies, the dead time becomes a larger percentage of the total period and account this loss in the total loss calculation. Another benefit of CoolSiC™ MOSFET over superjunction MOSFETs is that the dead time can be minimized to reduce this loss component because of the fast rise and fall times. The CoolSiC™ MOSFET channel turns on after the dead time, resulting in conduction loss. Losses during this mode of operation are calculated as:

Conduction loss

$$I_D := \sqrt{\frac{16}{3 \cdot \pi} \cdot \frac{P_{oPFC}^2}{V_{in_pk} \cdot V_{out}}} = 10.837\ A$$

Boost rectifier RMS current

$$P_{D_cond} := I_D^2 \cdot R_{dson} \cdot 1.2 = 10.146\ W$$

Conduction loss including $R_{DS(on)}$ temperature coefficient at 125°C

$$P_{revcond} := 2 \cdot I_{Lavg} \cdot V_{SD} \cdot DeadTime \cdot F_s = 1.603\ W$$

Conduction loss during dead time

$$P_{D_GD} := V_g \cdot Q_g \cdot F_s = 0.021\ W$$

Gate drive loss

Total loss as a rectifier

$$P_{D_tot} := P_{D_cond} + P_{revcond} + P_{D_GD} = 11.771\ W$$

Total loss per device over a full AC line cycle

$$P_{CoolSiC_tot} := \frac{P_{Q_tot} + P_{D_tot}}{2} = 9.438\ W$$

3.1.2 CoolMOS™ MOSFET selection

In a bridgeless totem-pole boost PFC, the diode bridge line rectifier is replaced by active switches, specifically superjunction MOSFETs, to eliminate the diode conduction loss. The only loss component in these devices will be the channel conduction loss. These devices operate at low line frequencies; therefore, switching losses are neglected.

$$R_{dsonSi} := 0.040\ \Omega$$

CoolMOS™ MOSFET on state resistance

$$I_{SiRMS} := \frac{P_{oPFC}}{\sqrt{2} \cdot V_{in_rms}} = 9.223\ A$$

RMS current at line frequency

$$P_{Sicond} := I_{SiRMS}^2 \cdot R_{dsonSi} \cdot 1.5 = 5.104\ W$$

Conduction loss of each line rectifying CoolMOS™ MOSFET at 125°C

3.1.3 PFC inductor design

The maximum amount of allowable ripple determines the required inductance. The amount of ripple also impacts the magnitude of differential and common mode conducted EMI, so it must be carefully chosen while keeping the overall size in mind. For this design, a ripple value of around 20% was chosen. The resulting inductance value obtained from calculations is 250 µH at full load and at the peak of the AC sine wave.

Hardware design considerations

As shown in Figure 8, this inductor is implemented using two stacked cores of Edge material from Magnetics, Inc., which has a permeability (μ) of 60 and an A_L of 61 nH/T^2. A two-layer winding of 60 turns provides the required inductance of around 250 μH under the above-mentioned conditions. The Edge material maintains its permeability over a wide range of DC bias and therefore is a great fit for PFC applications where minimizing inductance droop over the AC sinusoidal current is important. Compared to other powder iron cores, Edge material has significantly lower losses. These two crucial features help in designing a compact inductor for a high-density converter.

Figure 8 PFC inductor

The detailed calculation to understand inductance variation, core, and copper losses can be obtained from [2]. Figure 9 shows that the inductance varies from around 440 μH at no load to 260 μH at full load and peak of the AC line, satisfying the ripple requirements. The high inductance at no load and at AC zero crossing ensures a CCM operation, resulting in a high power factor, low total harmonic distortion, and low EMI across the entire line and load range.

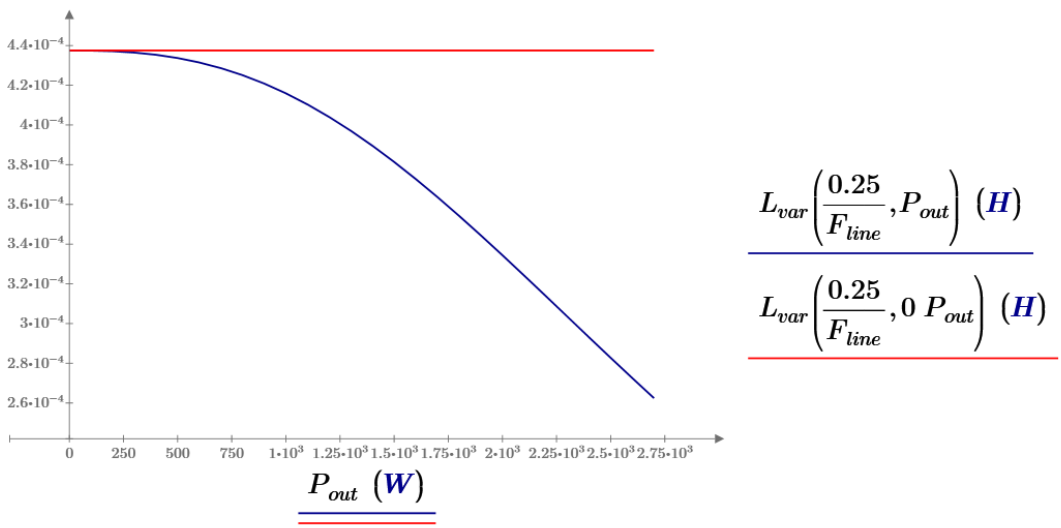

Figure 9 Inductance variation across the AC line cycle and load

The DC resistance of an assembled inductor is around 50 mΩ. This leads to a copper loss of 8.5 W at a maximum line current of 13 A. For this design, the core losses in the inductor at full load are around 1.6 W.

3.1.4 DC bus capacitors

The DC bus capacitor value is calculated based on two criteria: the maximum allowable double-line frequency ripple and the ability to hold up the bus voltage above a minimum value for at least 10 ms during an AC line drop-out condition. The greater of these two values must be selected to satisfy both conditions. In this design, two (2) 680 µF capacitors are selected to provide enough capacitance to satisfy the AC line drop-out requirements.

3.2 LLC DC-DC converter

The LLC resonant converter is a very popular topology in the server SMPS space due to its numerous advantages. It is an isolated soft switching topology where both zero-voltage switching (ZVS) and zero-current switching (ZCS) can be achieved to drastically minimize switching losses. The capability to operate with ZVS and ZCS provides many benefits. Soft switching reduces EMI significantly in the system. Reduced switching losses also mean that the converter can be operated at a high frequency, reducing the size of the transformer and capacitors to achieve high power density. Another benefit of this topology is that it can maintain soft switching over a wide range of loads, which enables high efficiency over the load range, satisfying the stringent OCP Titanium efficiency requirements as shown in Figure 10.

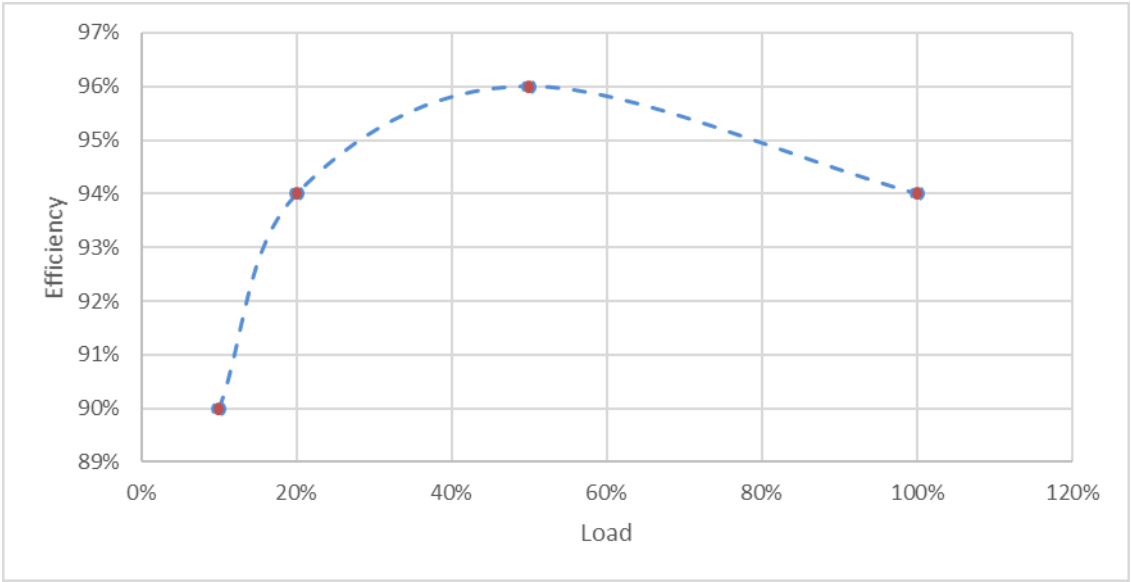

Figure 10 80 PLUS™ Titanium PSU efficiency requirement overload range

Despite the several performance benefits of the LLC resonant converter, adoption of this topology outside of the server space has been low due to challenges in designing the hardware and developing closed-loop controls. This application note shows that these challenges can be overcome and the high-performance benefits of this topology can be realized using Infineon products such as CoolMOS™ MOSFETs and XMC™ microcontrollers.

The process of hardware design and component selection for an LLC resonant converter is described in detail in [3] and [4]. The following sections will quantify the conduction and switching losses of the primary and

secondary MOSFETs. These loss numbers justify the selection of the MOSFETs in this design to meet the efficiency requirements as seen in the previous section.

3.2.1 Primary side CoolMOS™ MOSFET selection

With optimized dead time control, the LLC resonant converter can achieve soft switching for both turn-on and turn-off transitions over the majority of the operating range. This allows a designer to use cost-effective and high-performance CoolMOS™ MOSFETs. However, it is important to pay attention to a few parameters during the selection process to achieve a balance between low on-state resistance and low switching parasitics. In this aspect, CoolMOS™ MOSFET offers the best figure of merit to achieve both low conduction loss and soft switching. The device chosen for this design is the IPW60R024CFD7, which is a 600 V, 24 mΩ device with excellent switching characteristics. The comparison between different $R_{DS(on)}$ classes of CFD7 CoolMOS™ MOSFET in an LLC converter of similar power is shown in [4]. Based on the analysis, this 24 mΩ device is a good fit for this 2.7 kW LLC design.

LLC operating conditions

$Vin := 385\ V$ — Input DC voltage

$Vo := 12\ V$ — LLC output Voltage

$fsw := 90\ kHz$ — LLC resonant frequency

$P_{oLLC} := 2700\ W$ — Full load output power

$n := 15$ — Transformer turns ratio

Primary MOSFET conduction loss

$IpriFET_rms := 13\ A$ — Primary RMS current

$Rds_pri := 24 \cdot 10^{-3} \cdot \Omega \cdot 1.4 = 0.034\ \Omega$ — Primary switches on state resistance 75°C

$PpriFET_cond := IpriFET_rms^2 \cdot Rds_pri \cdot 2 = 11.357\ W$ — Primary switches conduction loss

Primary MOSFET body diode conduction loss

$Iturnoff := 12\ A$ — Turn-off RMS current

$Vf := 1\ V$ — Forward voltage of MOSFET body diode

$Tdeadtime := 200\ ns$ — Switch dead time

$Ppri_bodydiode := Iturnoff \cdot Vf \cdot Tdeadtime \cdot fsw \cdot 2 = 0.432\ W$

Hardware design considerations

Primary MOSFET turn off loss

$$Ppri_turnoff := \frac{Vin \cdot Iturnoff}{4} \cdot 40 \cdot ns \cdot fsw \cdot 2 = 8.316\ W$$

Primary MOSFET gate drive loss

$$Vdrv_pri := 12 \cdot V$$

Gate drive voltage

$$Qg_pri := 183 \cdot 10^{-9} \cdot C$$

Gate charge

$$Ppri_driving := Qg_pri \cdot Vdrv_pri \cdot fsw \cdot 2 = 0.395\ W$$

Total primary switch loss

$$Ppri_FET := PpriFET_cond + Ppri_bodydiode + Ppri_turnoff + Ppri_driving = 20.5\ W$$

3.2.2 Secondary side OptiMOS™ MOSFET synchronous rectifier

The optimum selection of MOSFETs for the secondary-side synchronous rectifier has been described in detail in [5]. The device selection depends primarily on minimizing and balancing both conduction and switching losses. Selecting a device with low $R_{DS(on)}$ to minimize conduction losses is critical due to the high output current in this design. As seen in the PFC design section, the switching loss comprises several loss components that arise from the switching transition characteristics of the device, such as the gate charge, turn on, and turn off energy. The OptiMOS™ 6 series of MOSFETs offers an excellent selection of low $R_{DS(on)}$ classes along with low parasitics, which minimize switching losses. The LLC converter operates mostly in a soft switching region, which inherently minimizes the switching loss. Due to this benefit, the designer has the freedom to select a low $R_{DS(on)}$ device to minimize conduction losses while still keeping switching losses low.

Secondary MOSFET loss calculation:

Secondary MOSFET conduction loss

$$Rds_sec := 0.7 \cdot 10^{-3} \cdot \Omega \cdot 1.5 = 0.001\ \Omega$$

Secondary switches on state resistance 75°C

$$IsecFET_rms := 174\ A$$

Secondary RMS current

$$PsecFET_cond := IsecFET_rms^2 \cdot \frac{Rds_sec}{8} \cdot 2 = 7.947\ W$$

Secondary switches conduction loss

Hardware design considerations

Secondary MOSFET body diode conduction loss

$Iturnon_SR := 25\ A$

Turn on current of the synchronous rectifier (SR) FETs

$Iturnoff_SR := 60\ A$

Turn off current of the SR FETs

$Vf_sec := 1\ V$

SR FETs diode forward voltage

$Tdiode_on := 400\ ns$

Diode conduction time between turn off and turn on

$Tdiode_off := 400\ ns$

Diode conduction time between turn on and turn off

$Psec_bodydiode := (Iturnon_SR \cdot Vf_sec \cdot Tdiode_on + Iturnoff_SR \cdot Vf_sec \cdot Tdiode_off) \cdot fsw \cdot 2 = 6.12\ W$

SR FETs body diode losses

Secondary MOSFET gate driving loss

$Vdrv_sec := 6 \cdot V$

SR FET gate drive voltage

$Qg_sec := \frac{118 \cdot 10^{-9} \cdot C}{10\ V} \cdot 6\ V = (7.08 \cdot 10^{-8})\ C$

SR FET gate charge

$Psec_driving := Qg_sec \cdot Vdrv_sec \cdot fsw \cdot 16 = 0.612\ W$

SR FET gate driving loss

Total secondary switch loss

$Psec_FET := PsecFET_cond + Psec_bodydiode + Psec_driving = 14.679\ W$

3.2.3 LLC transformer

The transformer material selection and construction are optimized to minimize AC and DC losses and achieve high power density. The primary consists of two 15-turn litz wire windings in parallel, and the center-tapped secondary consists of four 1-turn copper foil windings in parallel, as shown in Figure 11. The resonant inductor has a 6-turn litz wire winding.

Hardware design considerations

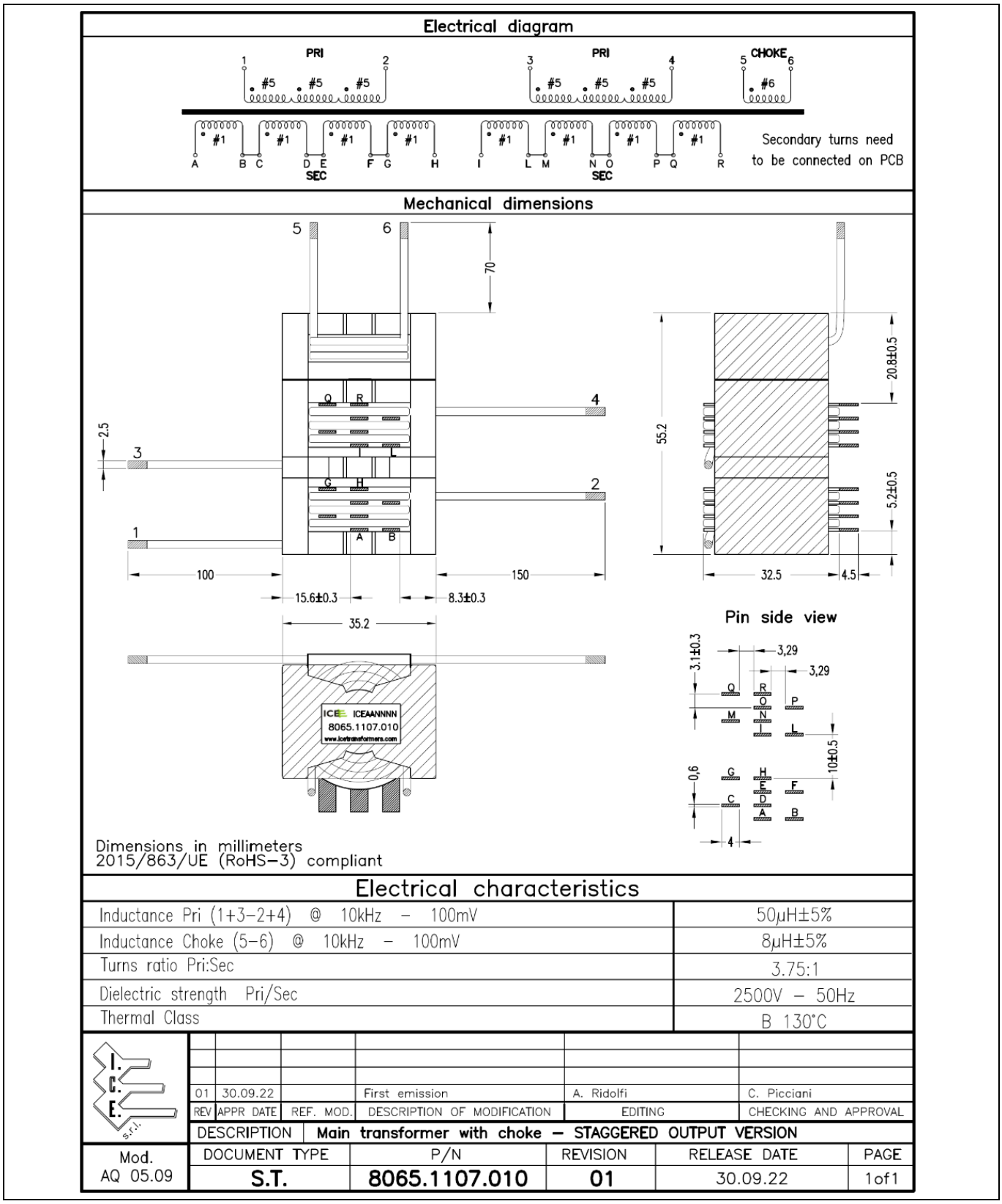

Figure 11 **LLC transformer schematic and dimensions**

Hardware design considerations

A FEA simulation was carried out to optimize the core and winding structure. Figure 12 shows the 3D model of the FEA simulation schematic of the transformer.

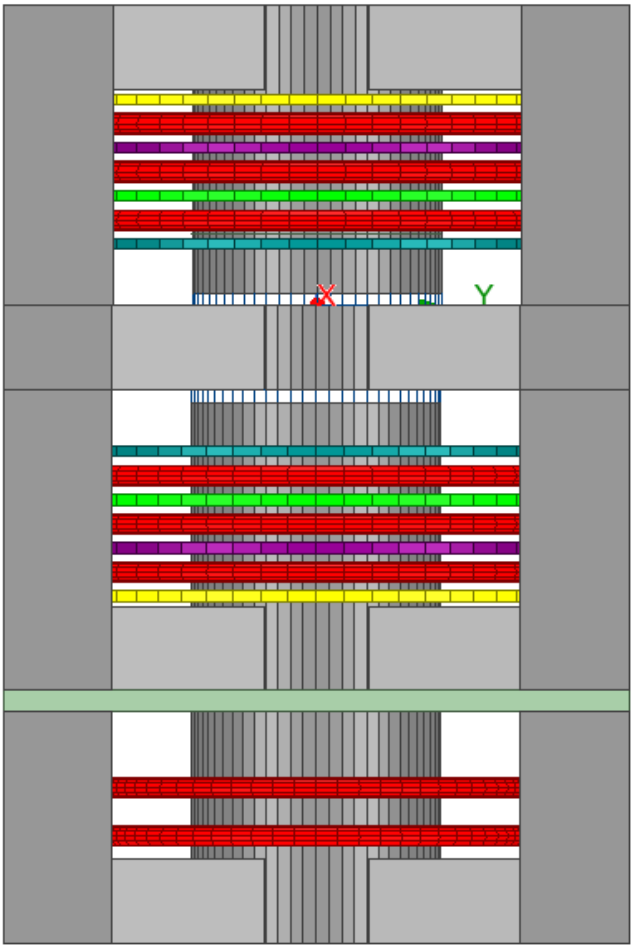

Figure 12 FEA simulation 3D model

This modeling and analysis are used to select the core structure that provides the lowest loss solution. As seen from the results of the FEA simulation in Figure 13, the optimized transformer design results in a total power loss of close to 22 W at the highest load condition.

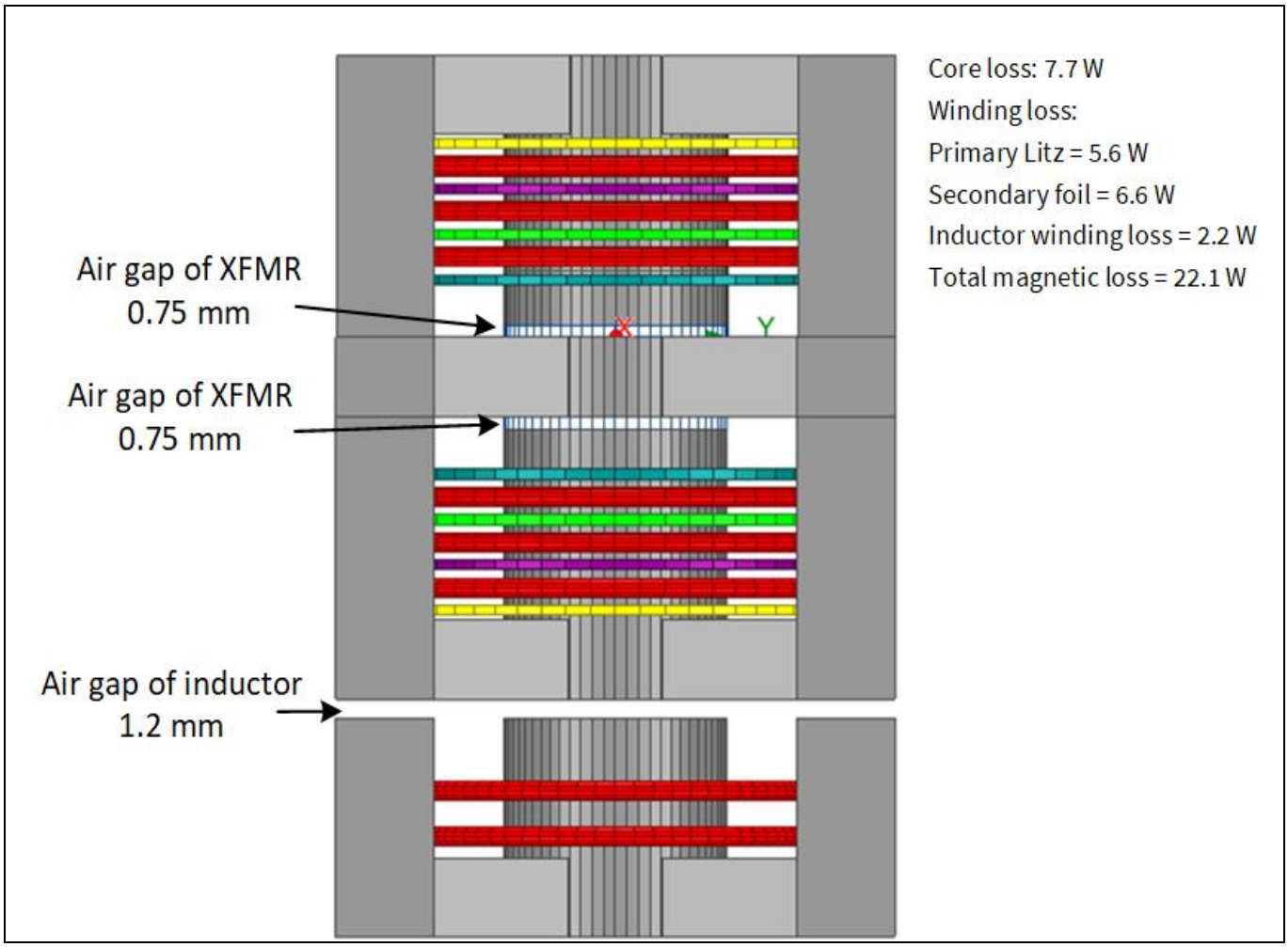

Figure 13 FEA simulation results

3.2.4 Oring FET

The primary criteria for selecting an Oring FET is low $R_{DS(on)}$, and in this design, the same FET that was used for synchronous rectification is chosen as the Oring FET.

Conduction loss in the Oring FET

$$PoringFET := \left(\frac{P}{Vo}\right)^2 \cdot \frac{Rds_sec}{8} = 6.645\ W$$

3.2.5 Losses in LLC capacitors

Loss in resonant capacitor

$$ICr_rms := 10\ A$$

LLC resonant capacitor RMS current

$$ESR_Cr := \frac{2 \cdot 10^{-3} \cdot \Omega}{3} = \left(6.667 \cdot 10^{-4}\right)\ \Omega$$

LLC resonant capacitor ESR

Hardware design considerations

$PCr := ICr_rms^2 \cdot ESR_Cr \cdot 2 = 0.133\ W$ Power loss in LLC resonant capacitor

Loss in output capacitor

$ICo_rms := 110\ A$ LLC output capacitor RMS current

$ESR_Co := \frac{2 \cdot 10^{-3} \cdot \Omega}{36} = (5.556 \cdot 10^{-5})\ \Omega$ LLC output capacitor ESR

$PCo := ICo_rms^2 \cdot ESR_Co = 0.672\ W$ Power loss in LLC output capacitor

Total capacitor losses

$Pcap := PCr + PCo = 0.806\ W$

An additional loss component is the termination, bus bars, and PCB trace loss due to the high output current. In this design, it is assumed to be around 15 W.

Figure 14 shows the estimated total losses in the LLC block at full load along with the loss breakdown.

$Ploss := Ppri_FET + Psec_FET + Pmag + PoringFET + Pcap + Pother = 79.729\ W$

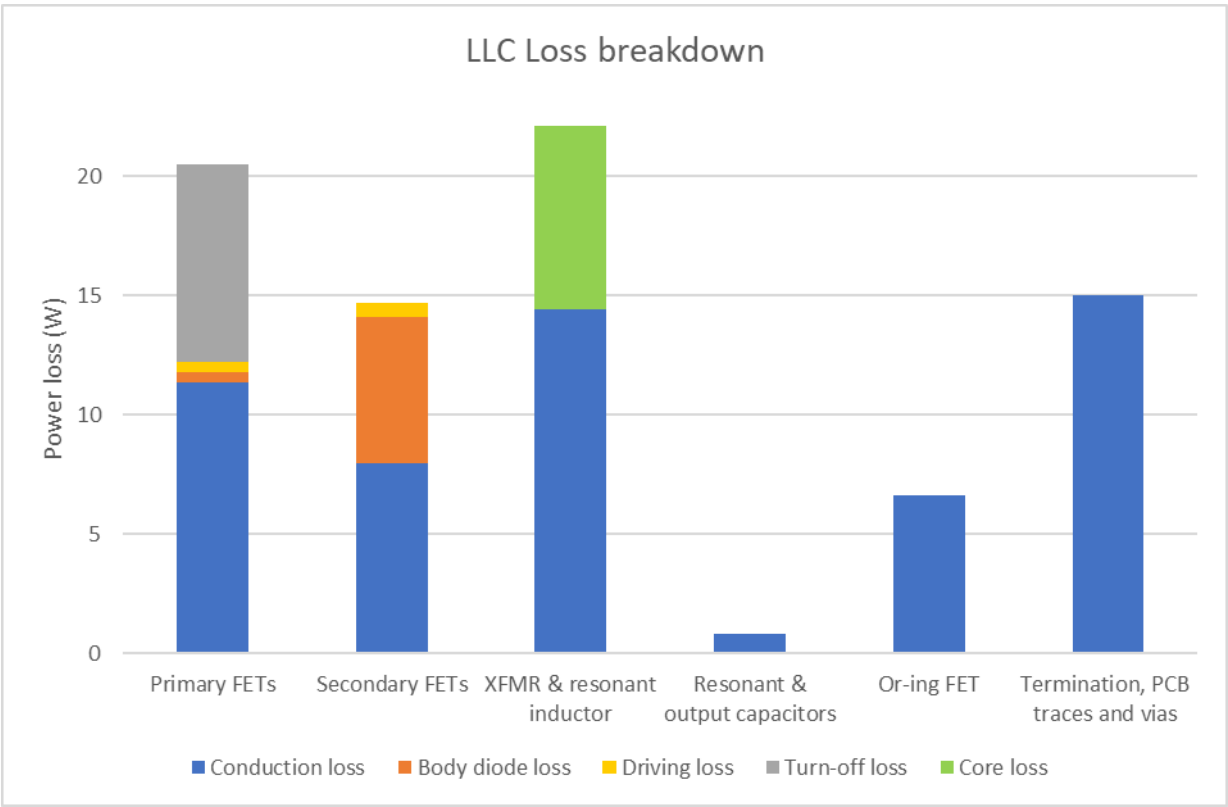

Figure 14 LLC loss breakdown

4 Control and firmware

4.1 PFC control

The structure of the PFC controller is shown in Figure 15. The goal of this controller is to regulate the PFC output voltage at the DC bus setpoint and control the input current shape so that a high-power-factor operation is achieved. This voltage must be regulated over line and load variations and controlled during transient events within a certain margin. This is achieved by first sensing the output voltage via hardware sensing and the ADC of XMC1404.

The output of the ADC is compared to the setpoint, and the error is fed to the PI controller, which generates the amplitude of the reference current. This current reference amplitude is multiplied by the instantaneous AC voltage to generate a sinusoidal reference for the average inductor current. This is compared against the measured average inductor current, and the error is the input to the inner current loop PI controller. The current PI controller uses the error to generate the closed-loop duty cycle value D_{CL}, which is then summed with the feed-forward duty cycle value D_{FF} to generate the final duty that shapes the inductor current as well as regulates the output voltage. The CCU8 timer uses this duty value to generate PWM signals used to drive the totem-pole PFC fast leg.

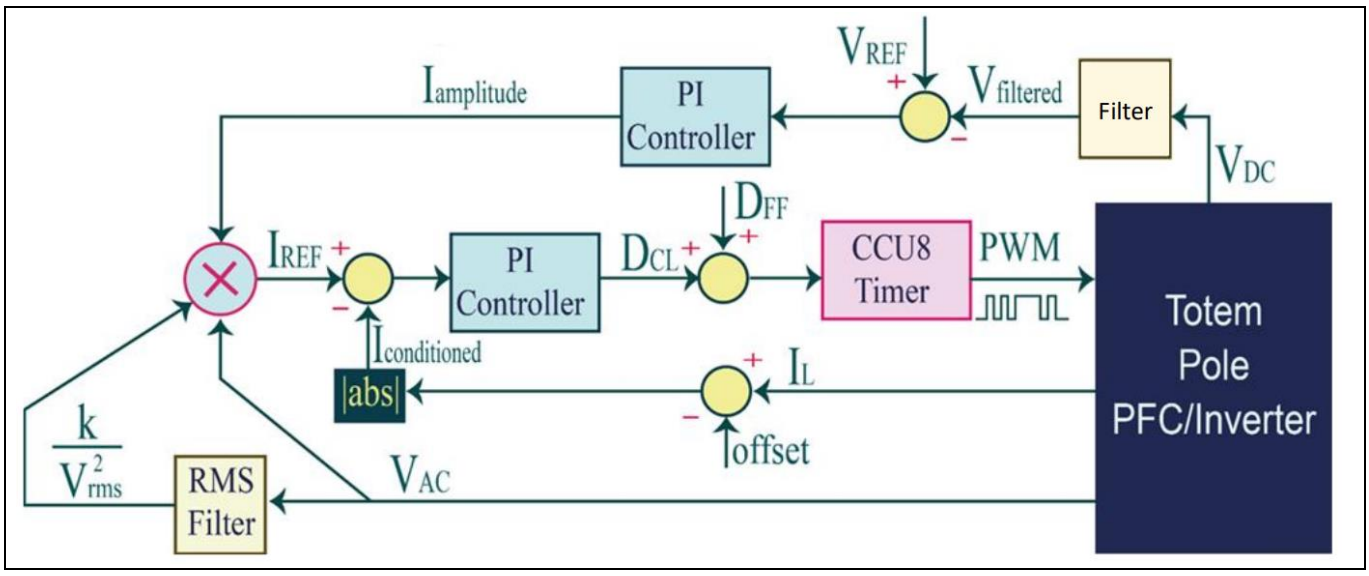

Figure 15 Control architecture of the bridgeless totem-pole PFC

Figure 16 depicts the digital implementation of the above architecture on the XMC1404 microcontroller. In the beginning, the MCU peripherals are initialized. The next step is to limit the inrush current during the charging of the DC bus capacitor. The relay is kept open for 300 ms to allow the inrush current to pass through an NTC and stay under the maximum limit. The relays are closed following this to bypass the NTC and eliminate the conduction loss during steady-state operation. The current sensor is then calibrated before the PWMs are enabled for a soft start to charge the DC bus capacitors to the final regulated voltage value. Both the voltage and current loops are implemented in one interrupt service routine (ISR).

Control and firmware

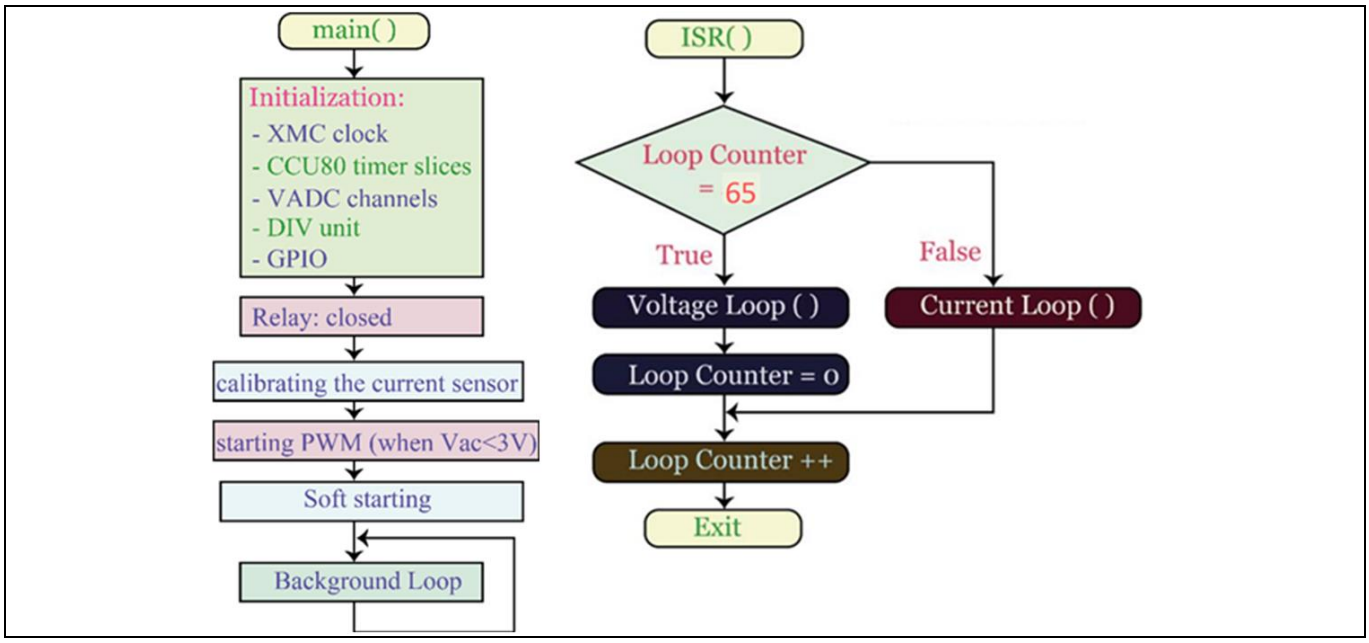

Figure 16 **Main control loop and interrupt service routine implemented in XMC1404**

4.1.1 Current control loop

The current and voltage measurements are captured once the current loop starts. The RMS value of the AC voltage is obtained by processing the measured AC voltage through an RMS filter. This value is used to determine the feed-forward duty cycle to counteract abrupt changes in AC voltage, thereby improving line regulation. The current loop difference equation is used to calculate the closed loop duty cycle and the feed-forward duty cycle, as shown in Figure 17. The voltage loop also uses the measured and filtered DC voltage to implement the voltage difference equation. The maximum and minimum duty cycle values are determined in this loop based on the instantaneous AC voltage and the allowed maximum and minimum DC voltages. This limits the peak overshoot and undershoot values of the voltage during load transients.

Control and firmware

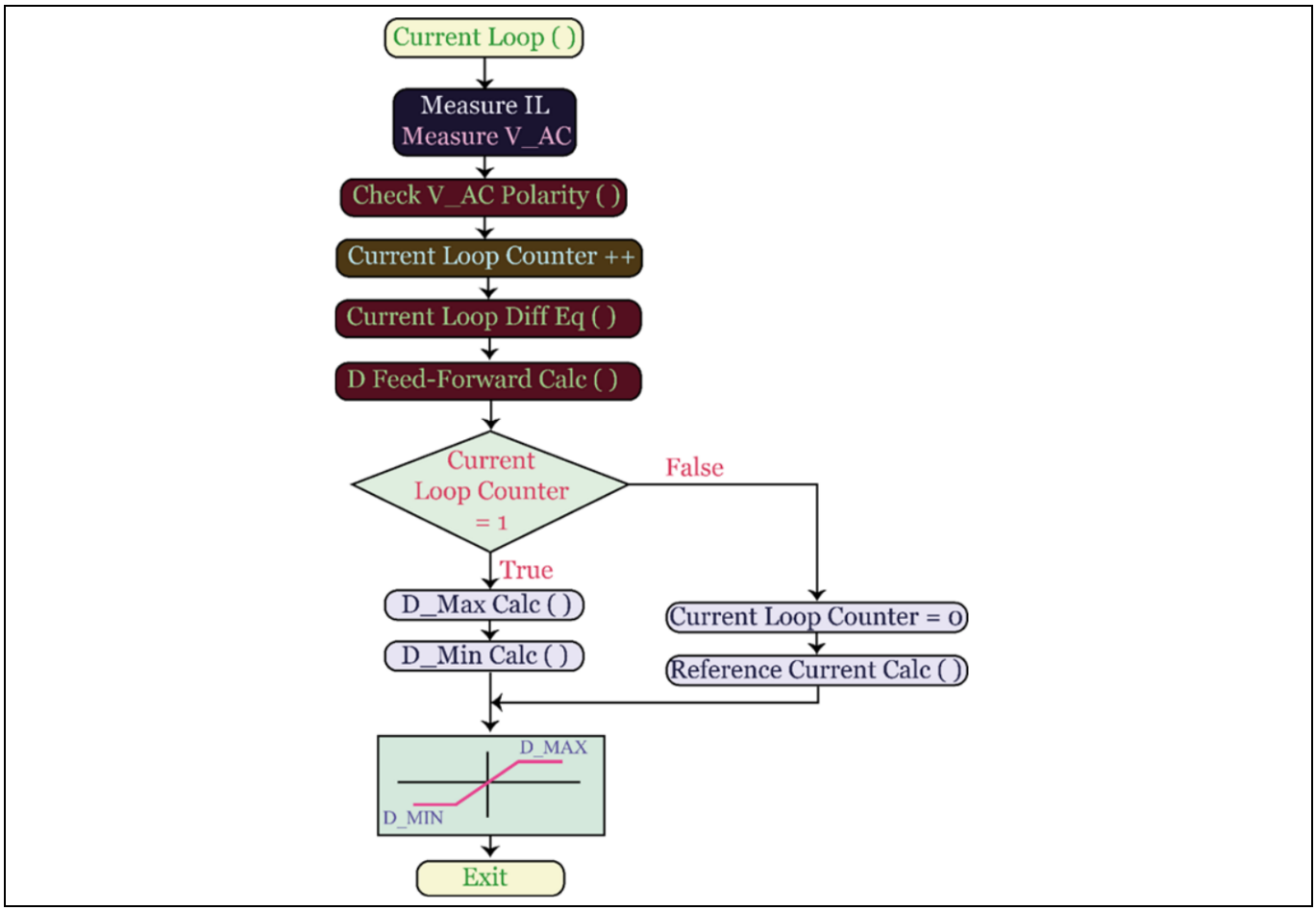

Figure 17 **Current control loop in XMC1404**

The controller also performs a zero calibration of the current sensing and measuring chain to cancel out any offset in the sensor, amplifier, and ADC signal chain. This is done by measuring 32 successive current samples during the zero crossing of 16 input voltage cycles. These values are averaged and used as a zero-current reference, as shown in Figure 18.

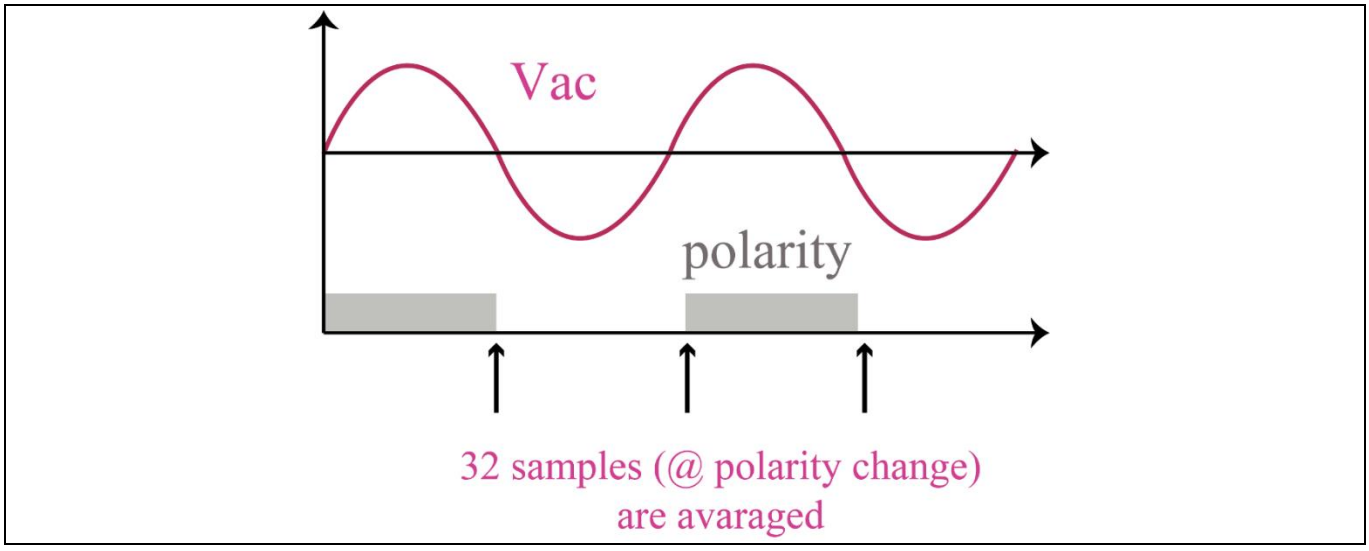

Figure 18 **Current sensor calibration**

Control and firmware

Figure 19 shows the digital implementation of the current controller. The final duty cycle is fed to the PWM timer CCU8. The main boost switch and the synchronous rectifier switch are determined based on the AC voltage polarity. Figure 20 shows the frequency response characteristics of the current controller. It has a gain crossover frequency of 4.5 kHz, and the phase margin is greater than 50°.

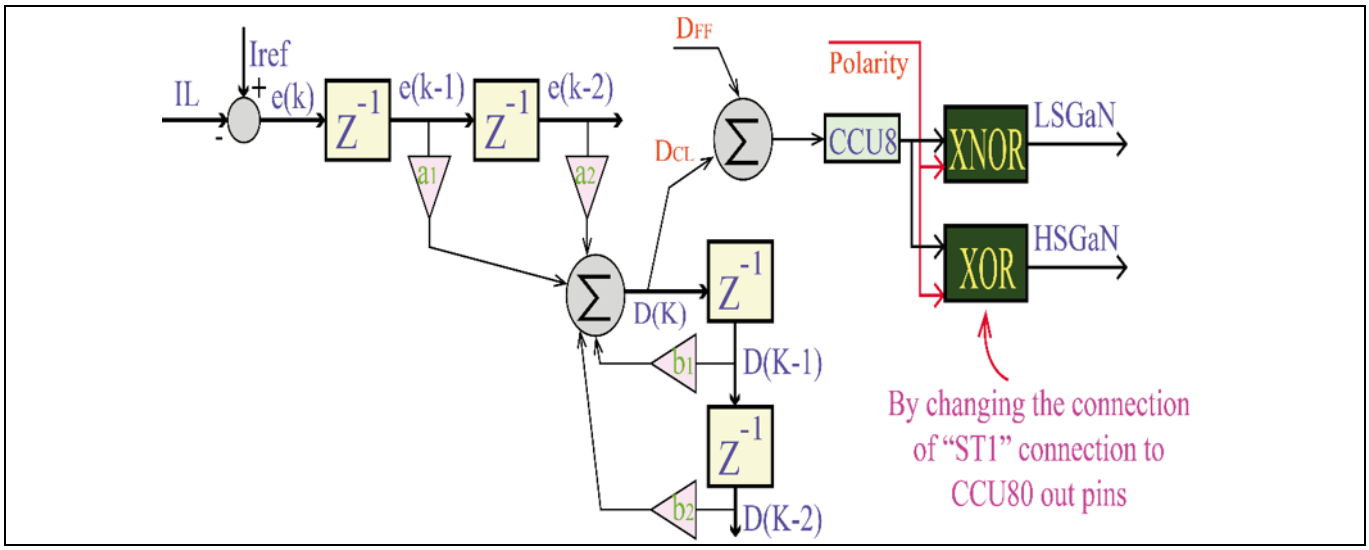

Figure 19 **Digital implementation of current control and compensation**

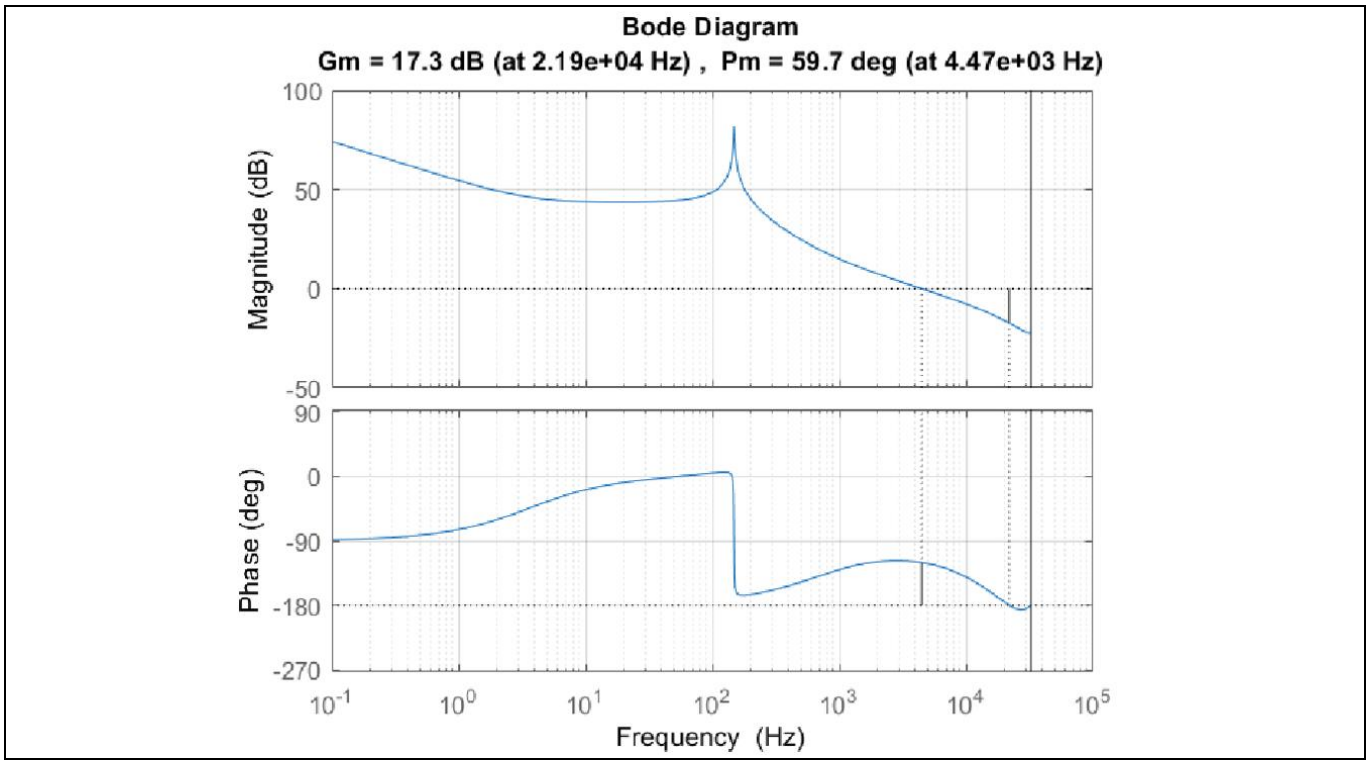

Figure 20 **Bode plot of current controller**

4.1.2 Control of the low-frequency half-bridge leg

The line frequency half-bridge switches change state during every zero crossing of the AC cycle. This is determined by measuring the AC voltage and comparing it with a threshold set near zero. A timing hysteresis is utilized to ensure smooth and accurate switching without any jitters. The high-frequency leg is also disabled during the short transition period when the line-frequency leg commutates.

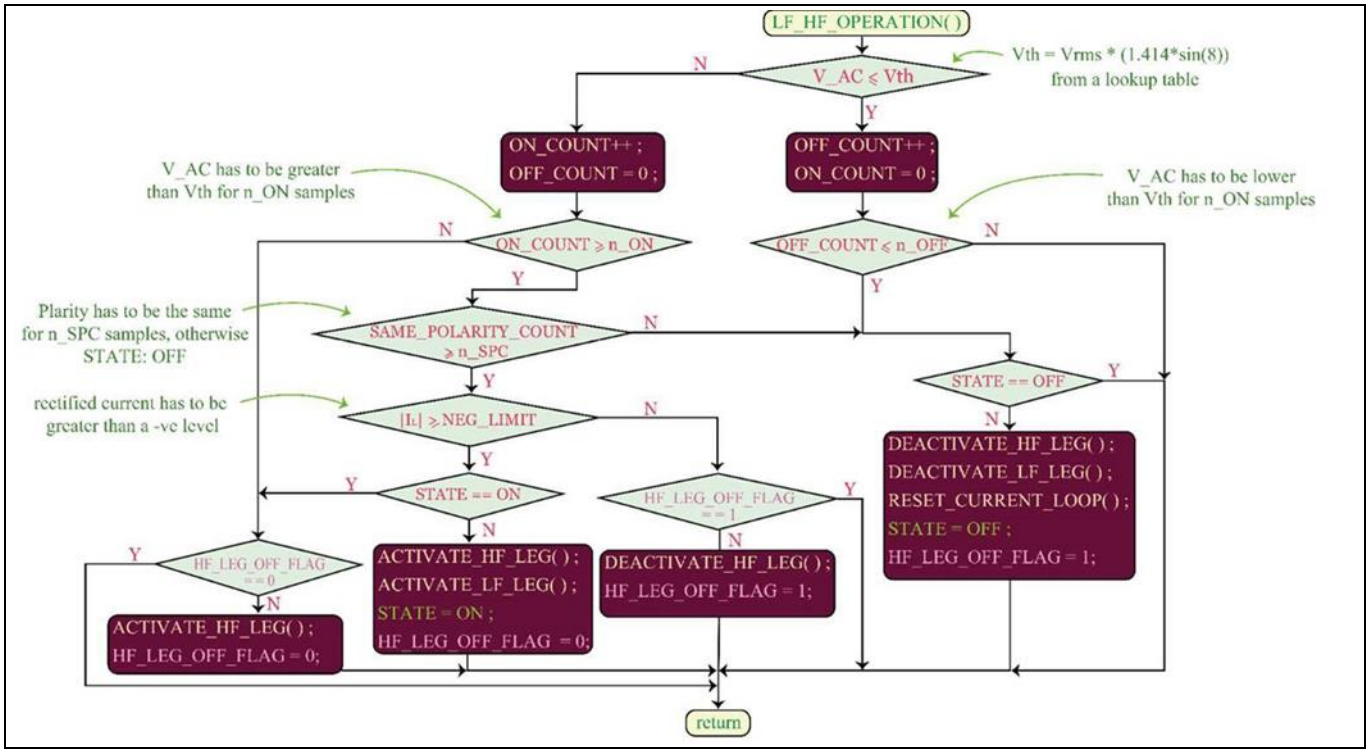

Figure 21 State-diagram for the control of the low-frequency half-bridge leg

Figure 22 shows the operating waveforms of the line frequency half-bridge leg.

Control and firmware

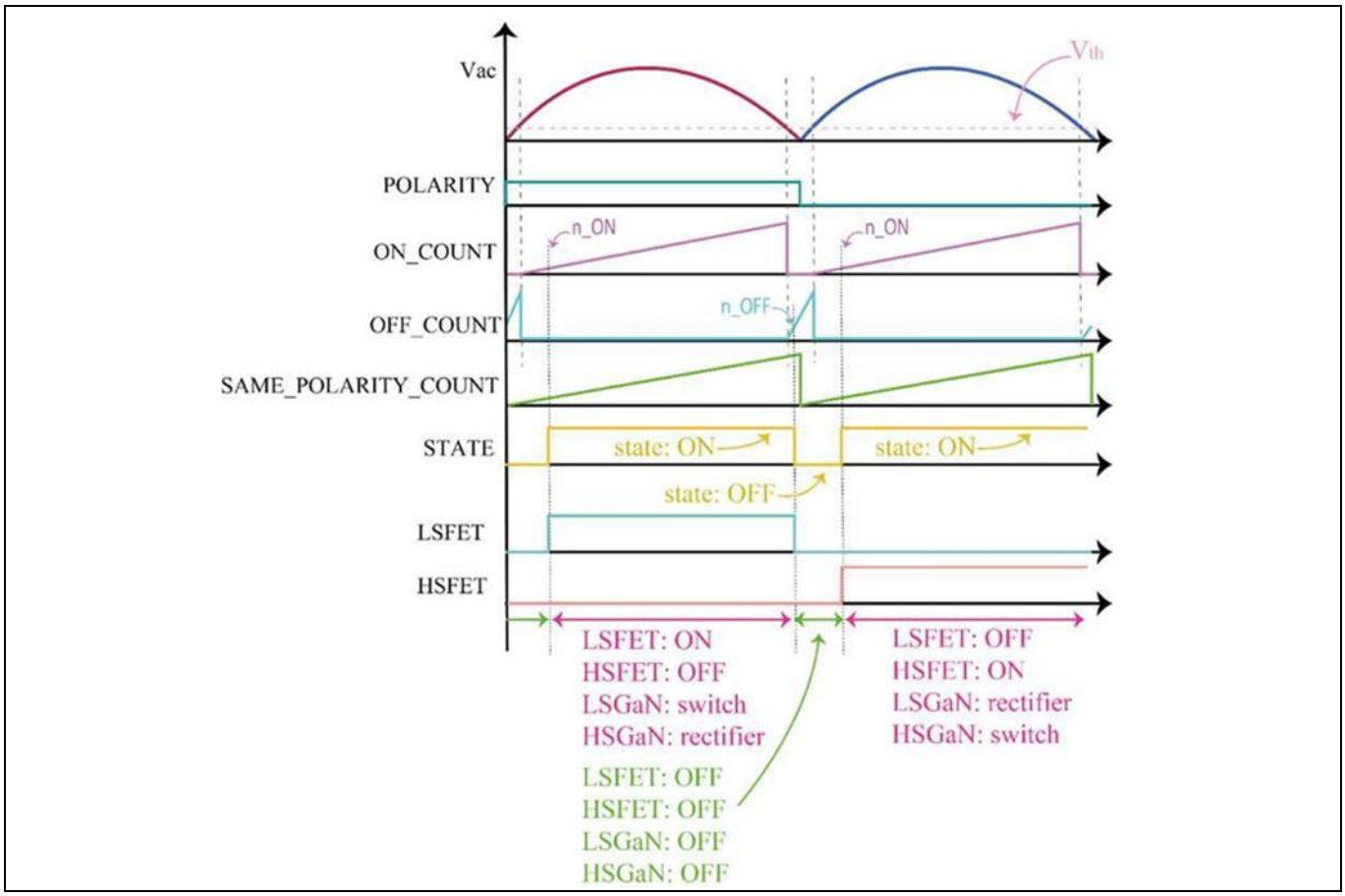

Figure 22 **Operating waveforms for the control section of the low-frequency half-bridge leg**

4.1.3 Voltage control loop

The flow of the outer voltage control loop is shown in Figure 23, and the digital implementation is shown in Figure 24. It has a gain crossover frequency of 10 Hz in order to not react to the line frequency component of the output voltage. It has a phase margin greater than 50°, as shown in Figure 25.

Control and firmware

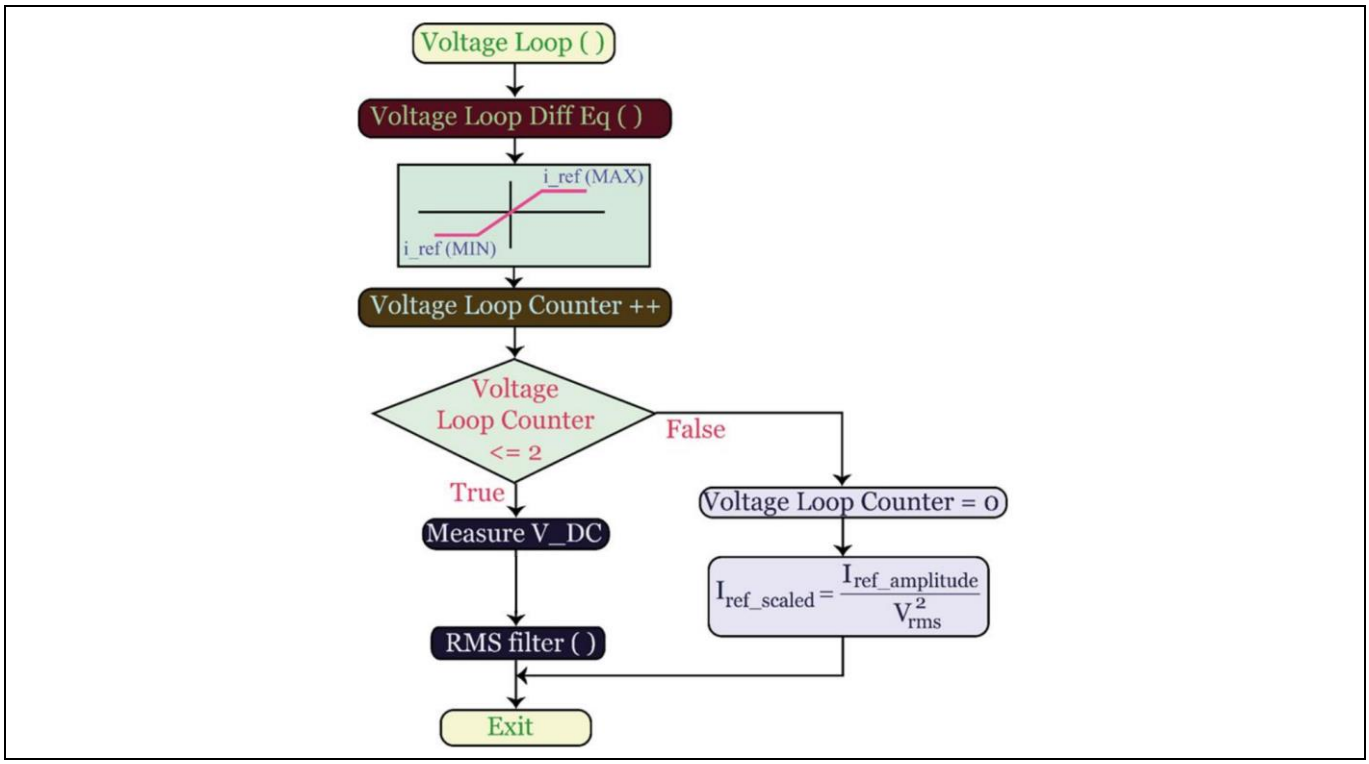

Figure 23 **Voltage control loop in XMC1404**

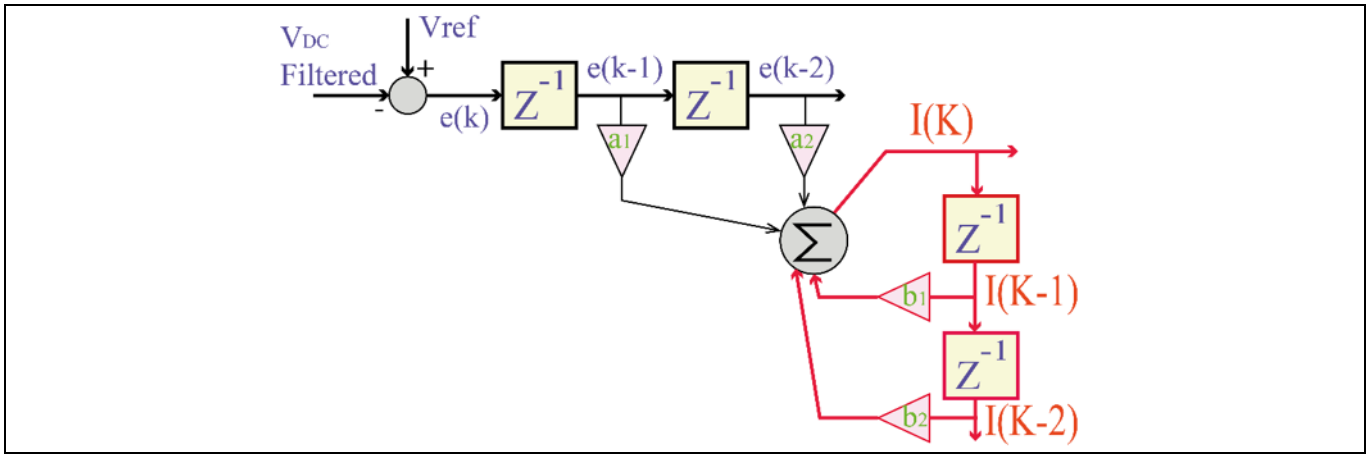

Figure 24 **Digital implementation of voltage control and compensation**

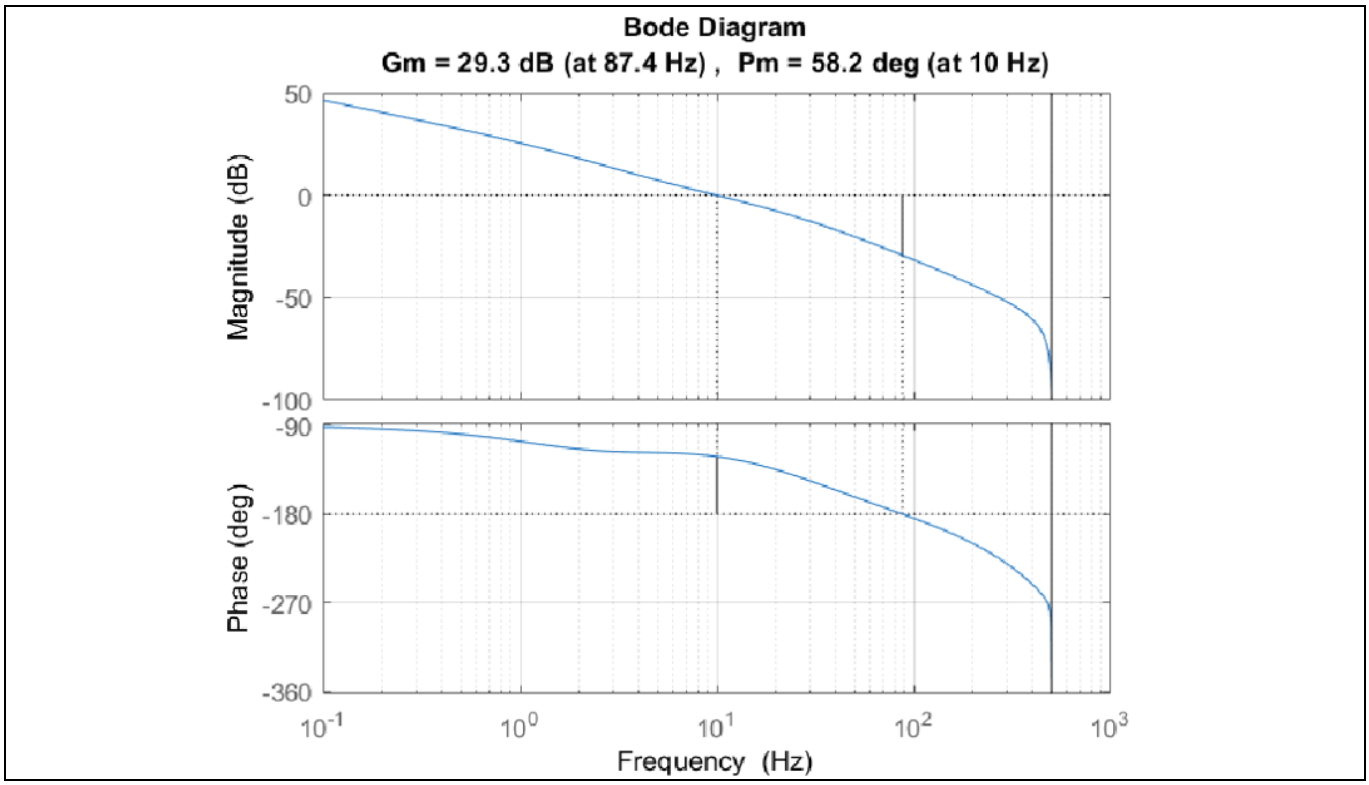

Figure 25 Bode plot of voltage controller

4.2 LLC control

Figure 26 shows the structure of the LLC controller. The goal of this controller is to regulate the output voltage to the setpoint under all line and load conditions during steady-state and transient operations. This is achieved by first sensing the output voltage and comparing it to the setpoint. The resulting error is then passed on to type 3 and the lag compensator. The compensator outputs a delta period, which is appended to the minimum period, resulting in the final LLC period. This period is fed to the CCU8 timer of the XMC4200 microcontroller, which generates the PWM signals for the LLC power stage.

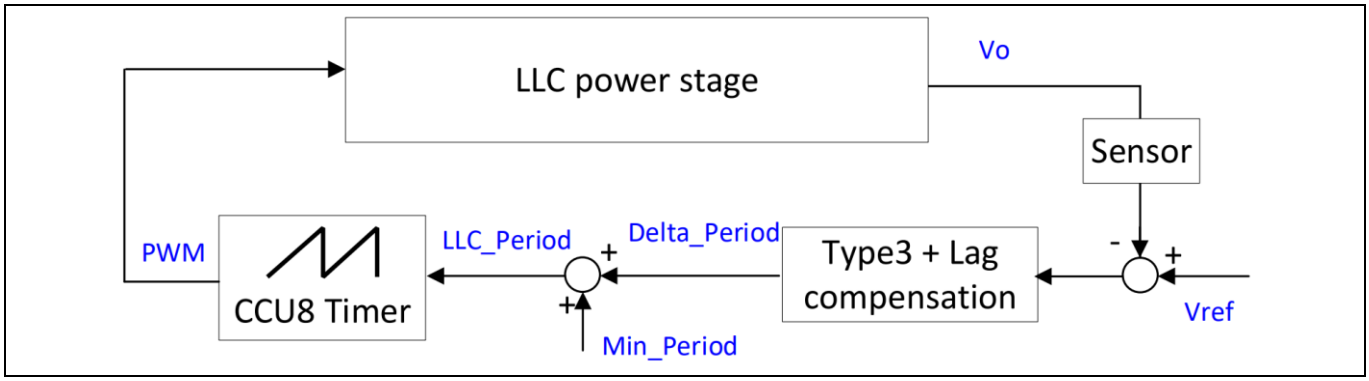

Figure 26 Control architecture of LLC converter

Figure 27 shows the digital implementation or flow of the controller. At startup, the DC bus voltage is checked to ensure that it is greater than the turn-on threshold. Once confirmed, the reference voltage is ramped up from 0 to 12 V. A slow PI controller is used during startup. At the beginning, the PI controller is saturated, and the initial switching frequency is limited to the maximum frequency. Then the switching frequency starts

decreasing as Vref increases. Only primary PWM is turned on during the Vref ramp. When the measured output voltage rises close to a threshold (for example, 11.6 V), a soft start of SR PWM happens. SR on time gradually ramps from zero to the maximum value, which is half the resonance period when below resonance or half the switching period when above resonance with some delays.

This LLC controller is executed in an interrupt service routine running at a rate of 30 kHz. Other functions are also included in this ISR, such as burst mode, decisions on starting or stopping operations, and communication.

Figure 28 shows the digital implementation of the Type 3 + lag compensation controller. The additional lag compensation is to reduce the double-line frequency ripple component, which comes from the PFC, in the output voltage. Figure 29 shows the frequency response of the LLC controller.

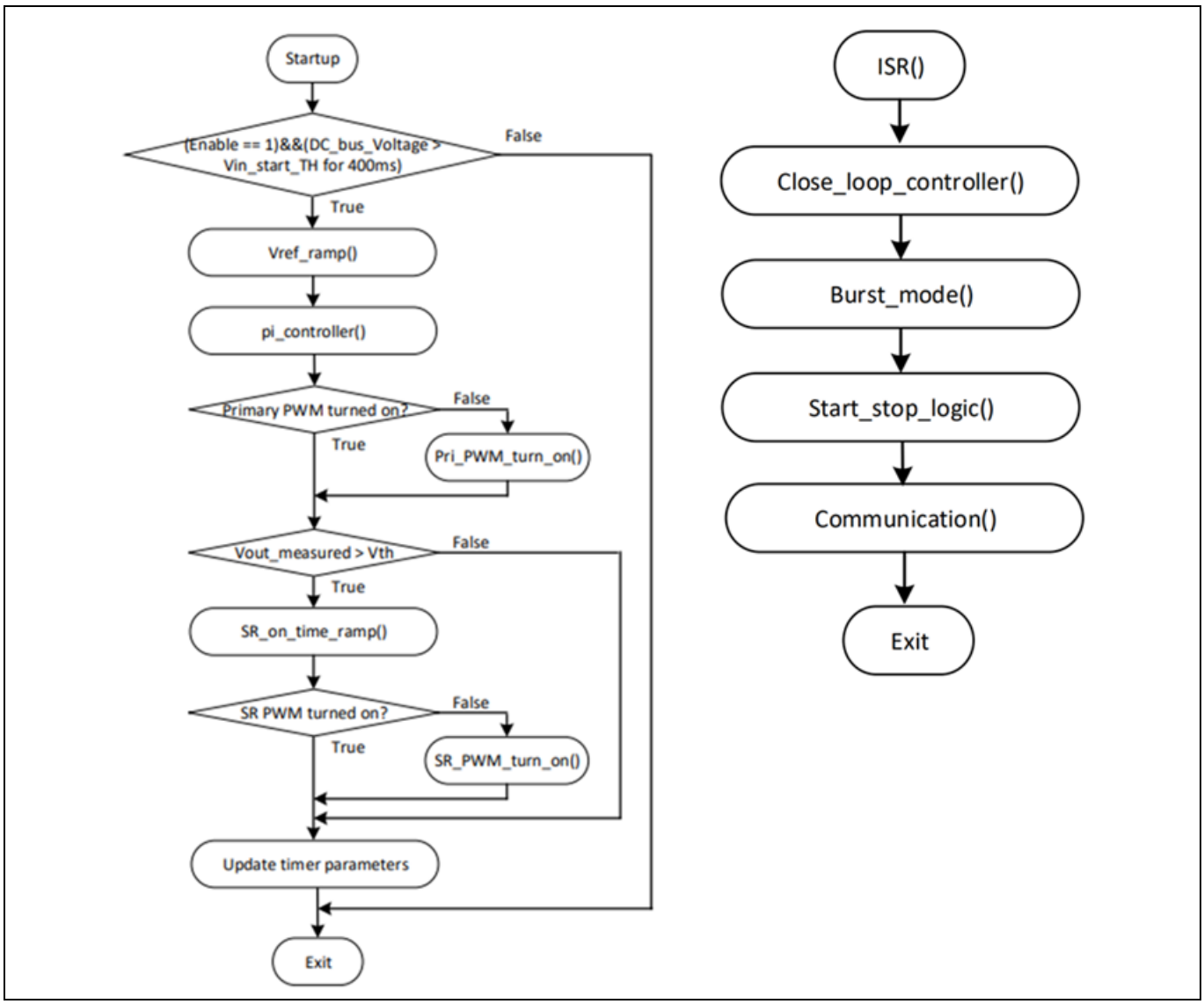

Figure 27 **Main control loop and the interrupt service routine (ISR)+**

Control and firmware

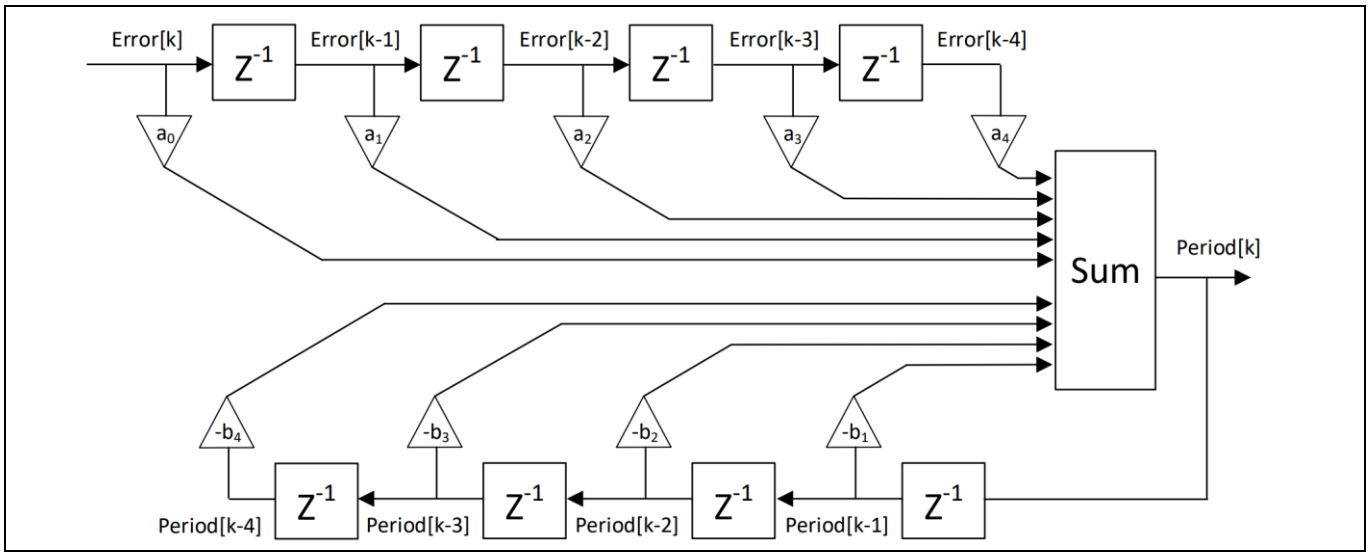

Figure 28 **Digital implementation of type 3 + lag compensation**

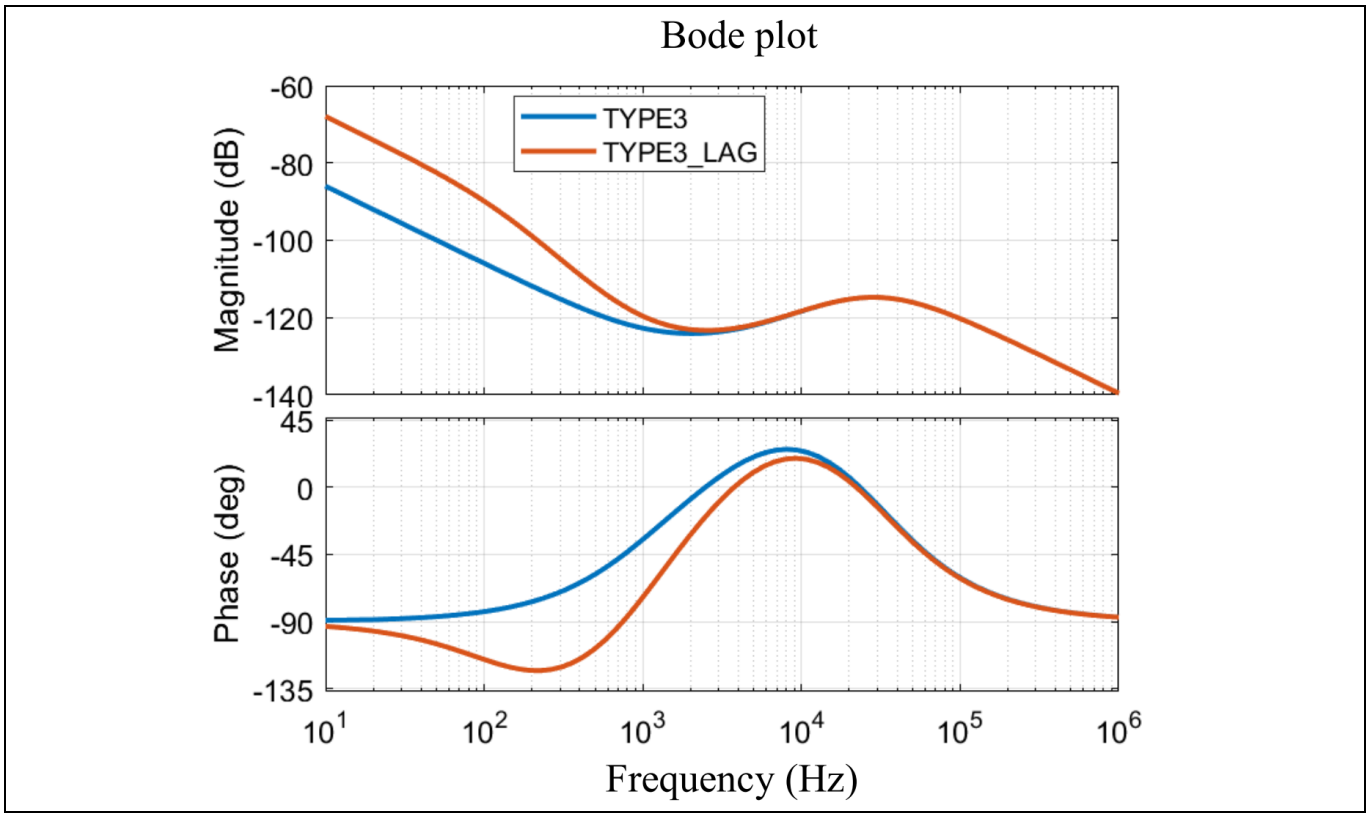

Figure 29 **Bode plot of LLC controller**

4.3 Protection features

The PFC and LLC circuit blocks are protected against failures due to electrical and thermal overstress. Critical signals are sensed through instrumentation and input to the ADC channels of the two microcontrollers. A failure is detected when the ADC output exceeds the set threshold. The protection features, thresholds, and responses are listed in Table 5.

Table 5 Protection features

Protection	Protection threshold
PFC protections	
AC overvoltage	275 V_{rms}
AC overcurrent	32 A_{pk}
Output overvoltage	435 V
LLC protections	
Input undervoltage	300 V
Primary overcurrent	40 A_{pk}
Over temperature	~120°C
Output overvoltage	15 V

5 Test results

The PSU was tested extensively to validate the electrical performance over steady-state and transient operating conditions as defined in the requirement specifications.

Figure 30 shows the PSU operation at steady-state output. The AC-coupled output voltage waveform shows a ripple of 176 mV_{pp}, which is below the maximum allowed limit. This validates a stable hardware and control loop design to achieve regulated output voltage with low ripple.

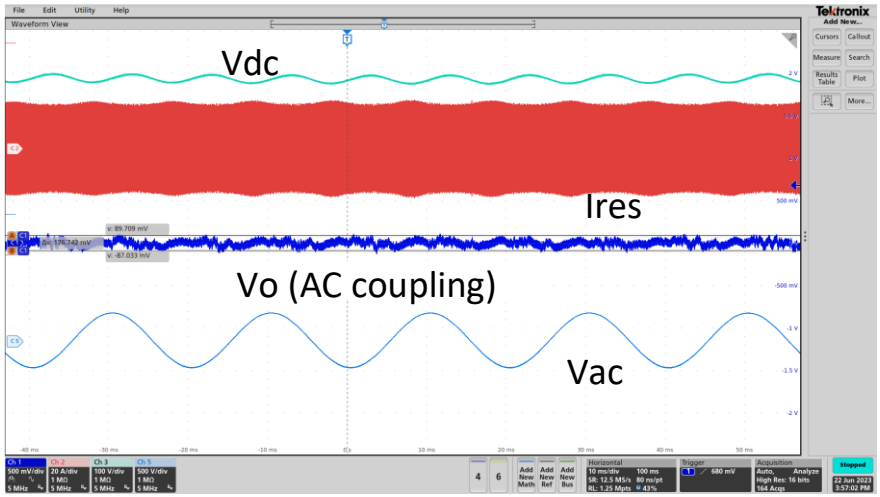

Figure 30 Steady state output voltage ripple (test condition: Vac = 230 V, f = 50 Hz, full load)

Figure 31 shows the startup performance under no load conditions. As seen, the converter starts up with a minimum overshoot at the output, which settles and regulates in a short amount of time. There is a short period of PWM shutdown caused by burst operation due to the no-load condition. Figure 32 shows the same operation at full load conditions with excellent control of the output voltage without any operation abnormalities. These waveforms show the performance of the digital controller for the two stages, implemented with the XMC™ microcontrollers, providing stable control during transient operation.

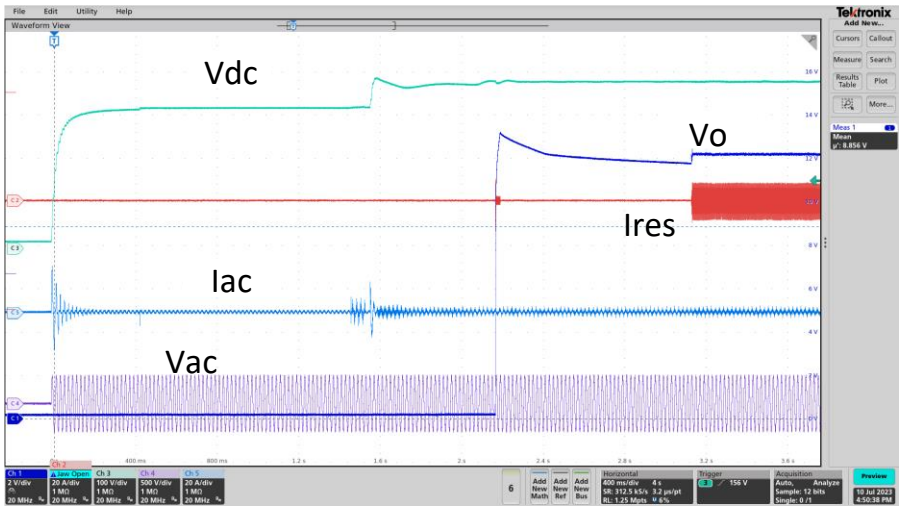

Figure 31 Startup at no load (test condition: Vac = 230 V, f = 50 Hz)

Test results

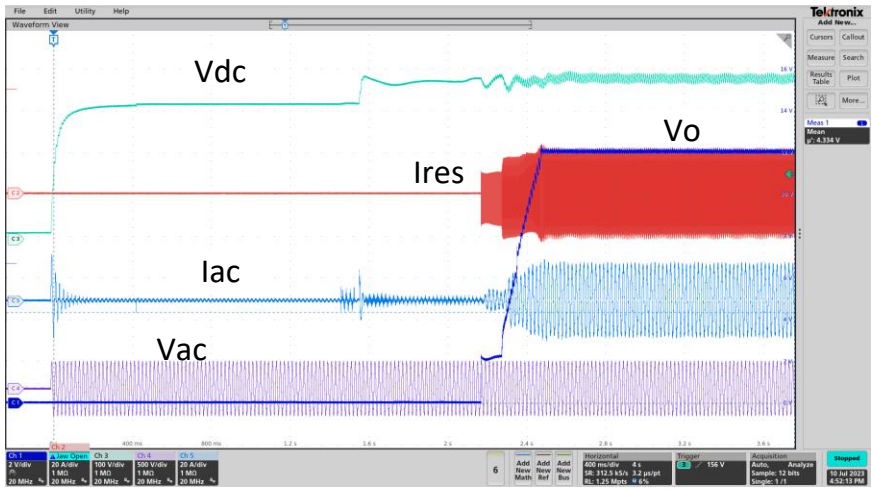

Figure 32 **Startup at full load (test condition: Vac = 230 V, f = 50 Hz)**

Continuing with transient operation, Figure 33 shows the testing of the PSU during load steps from 5% to 105%, during which the output voltage overshoots and undershoots must be limited below 1.3 V. As seen in the waveform, the output voltage overshoot and undershoot are below 1 V, which meets the regulatory requirements under this operating condition.

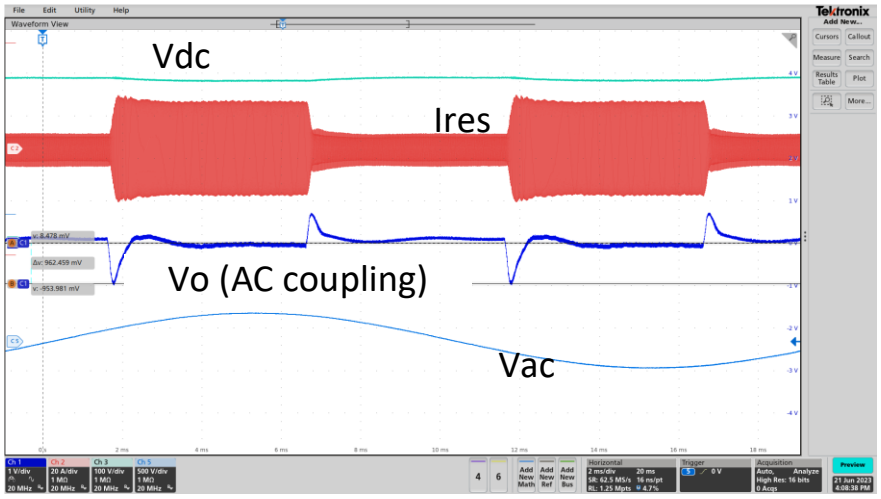

Figure 33 **Transient operation (test condition: Vac = 230 V, f = 50 Hz, 5% load to 105% load, 2.5 A/us slew rate)**

In server applications, the operation of the PSU under abnormal line conditions is critical in maintaining regulated power for the downstream loads. One of the requirements is to provide output voltage and power within the specified limits during AC line drop-out conditions. The regulations state that the PSU must continue to provide regulated output for the duration of the AC line dropout of at least 10 ms. Figure 34, Figure 35, and Figure 36 show the PSU output voltage performance during AC line drop-out conditions at 0-, 45-, and 90-degree angles of the AC voltage. The output voltage undershoot and overshoot are well controlled during this operation.

Test results

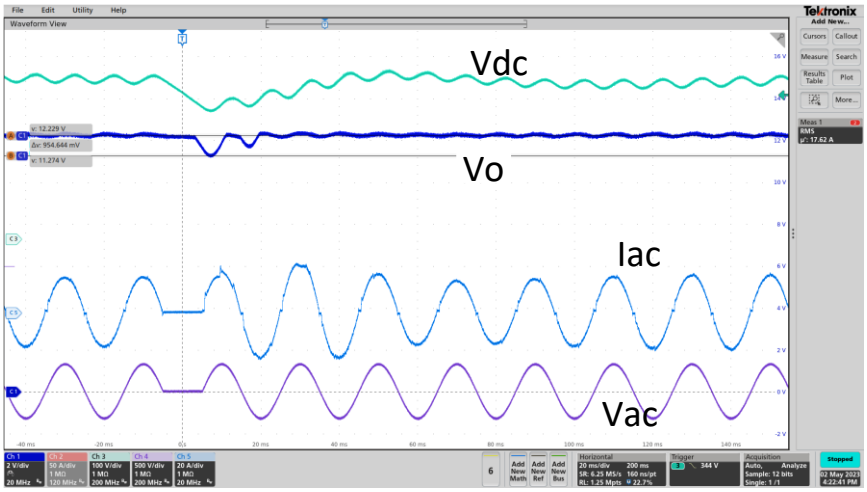

Figure 34 **10 ms AC line dropout (test condition: Vac = 230 V, f = 50 Hz, full load, line dropout at 0 degree angle)**

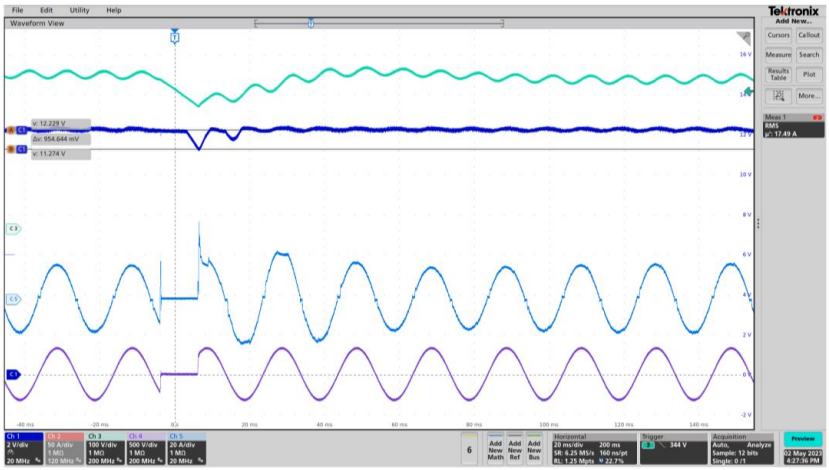

Figure 35 **10 ms AC line dropout at 100% load (test condition: Vac = 230 V, f = 50 Hz, full load, line dropout at 45 degree angle)**

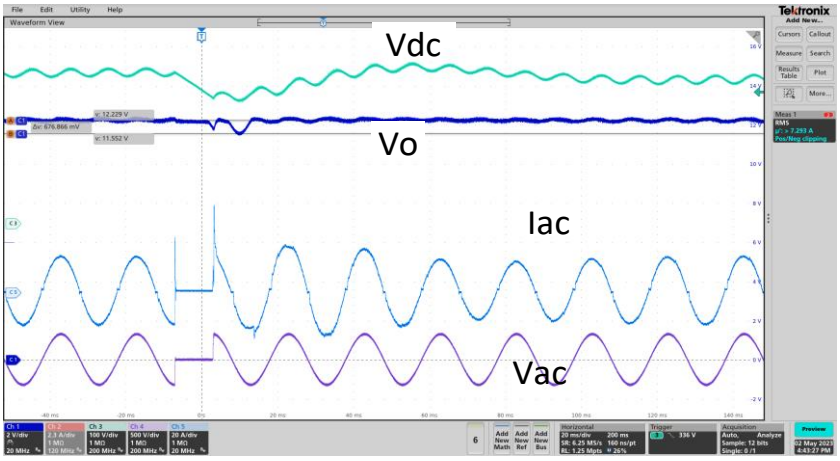

Figure 36 **10 ms AC line dropout at 100% load (test condition: Vac = 230 V, f = 50 Hz, full load, line dropout at 90 degree angle)**

Test results

Figure 37 shows the thermal performance of critical components at full load. The temperatures are well below the absolute maximum limits of the components, demonstrating the high electrical efficiency and optimum thermal design of the PSU.

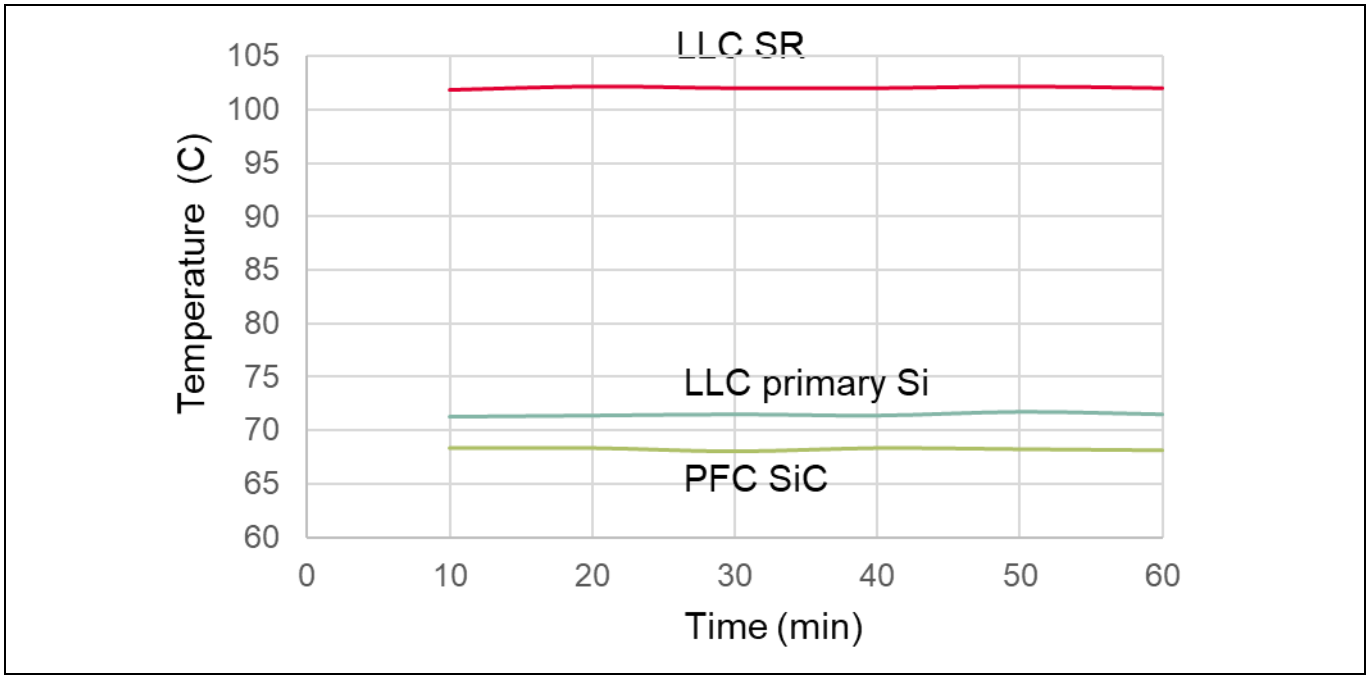

Figure 37 **Thermal measurements within the enclosure (test condition: Vac = 230 V, f = 50 Hz, full load)**

Table 6 shows the electrical performance of the PSU at different load points at 230 V input and full load. The output voltage is regulated very tightly over the load range.

Table 6 **Electrical performance at 230 V, 50 Hz input**

Load	VAC (V_{rms})	IAC (A_{rms})	PAC (W)	Vout (V)	Iout (I)	Pout (W)	Eff (%)	Ploss (W)
10%	229.485	1.3778	299.28	12.1883	22.426	273.34	91.33%	25.94
20%	229.335	2.5535	578.6	12.1801	44.957	547.58	94.64%	31.02
30%	229.198	3.7627	858.23	12.1716	67.488	821.43	95.71%	36.8
40%	228.976	4.9943	1140.81	12.1662	90.027	1095.29	96.01%	45.52
50%	228.853	6.2369	1425.36	12.16	112.661	1369.96	96.11%	55.4
60%	228.732	7.4882	1711.2	12.151	135.098	1641.58	95.93%	69.62
70%	228.644	8.7578	2000.82	12.1507	157.63	1915.31	95.73%	85.51
80%	228.515	10.0408	2292.99	12.1541	180.176	2189.88	95.50%	103.11
90%	228.393	11.3092	2581.61	12.1579	202.207	2458.42	95.23%	123.19
100%	228.296	12.6563	2887.96	12.1611	225.255	2739.36	94.86%	148.6

To qualify as an 80 PLUS™ Titanium server PSU, the design must exceed the efficiency requirements at specified load points, as shown in Table 3. Figure 38 shows that this design meets and exceeds the efficiency requirements. Figure 39 shows that the PSU harmonic emissions are below the IEC 61000-3-2 requirements for maximum harmonics injected back into the AC line.

Test results

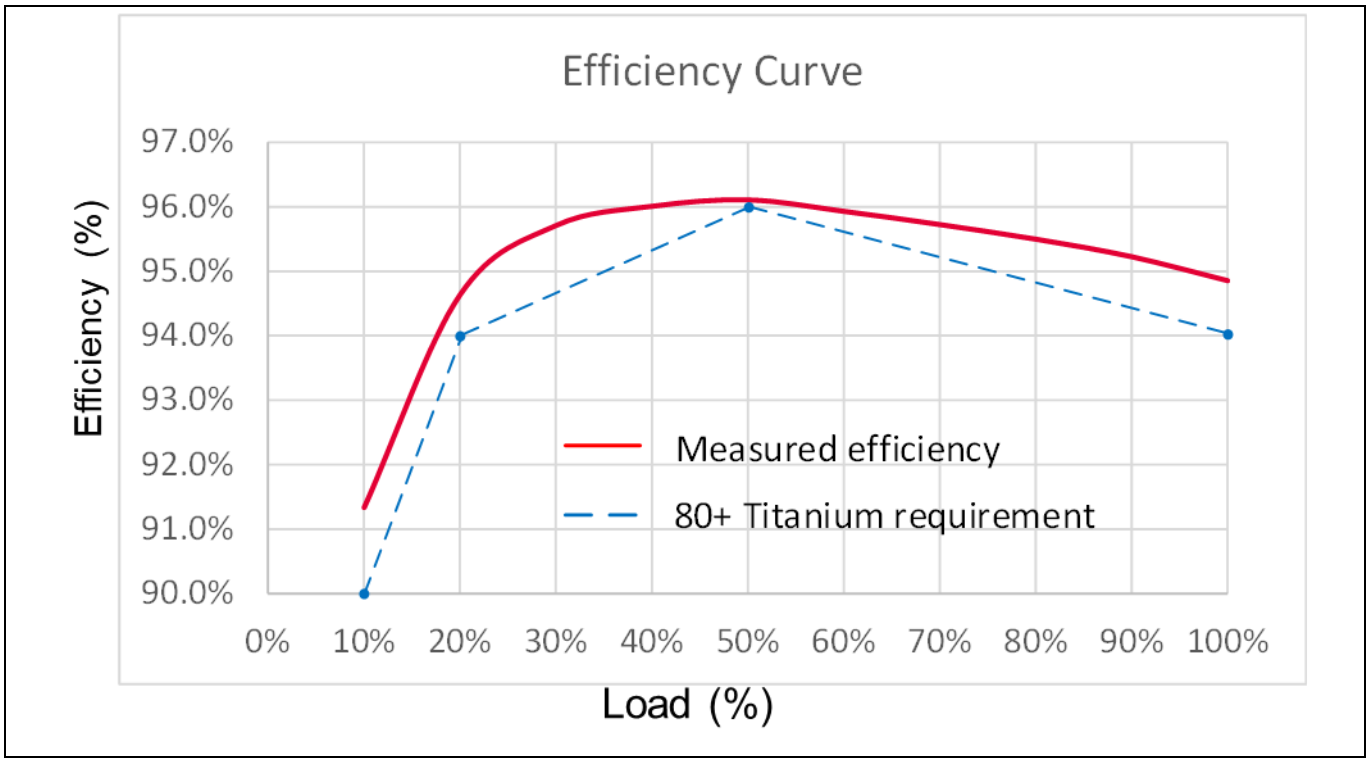

Figure 38 **Converter efficiency at 230 V AC input**

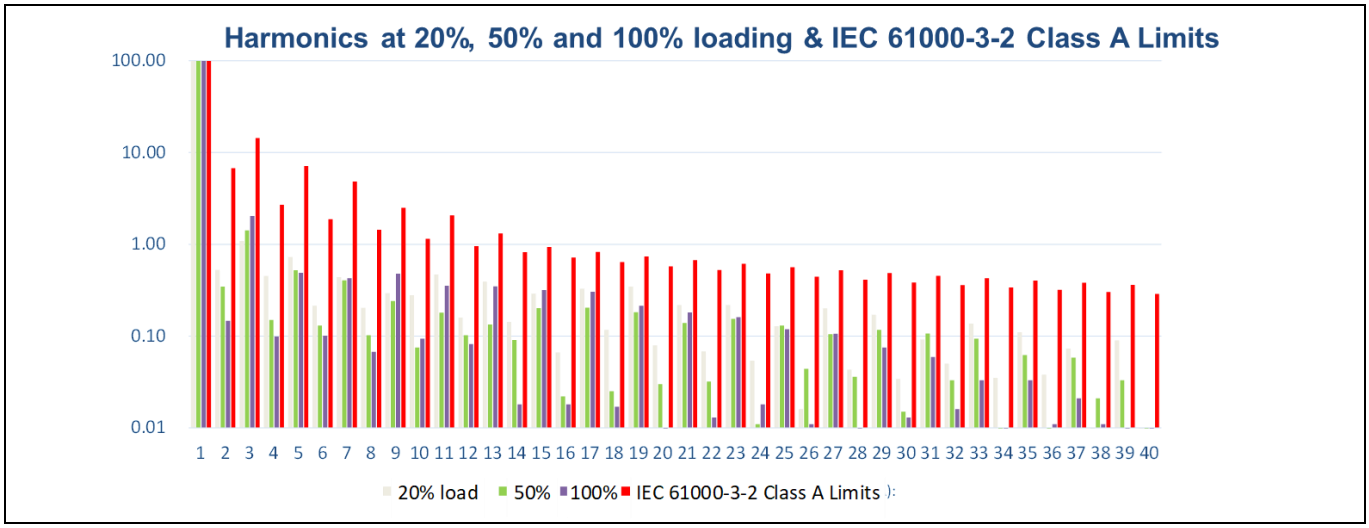

Figure 39 **Harmonics measurement of the converter compared to IEC 61000-3-2 limit**

6 Summary

This application note introduces a 2.7 kW enterprise server PSU implemented with Infineon's industry-leading products. It achieves a peak efficiency of 96.11% and a low harmonic content to meet the stringent requirements. Excellent electrical and thermal performances are achieved by using best-in-class CoolSiC™ and CoolMOS™ MOSFETs in the PFC and LLC blocks. The high power factor and excellent power quality of the totem-pole PFC are achieved through digital control using XMC1404. The LLC achieves tight regulation and excellent transient load performance using the XMC4200 for digital control.

Test results show compliance with target specifications and regulations to meet the 80 PLUS™ Titanium standards.

7 Detailed schematics

7.1 Main board schematic

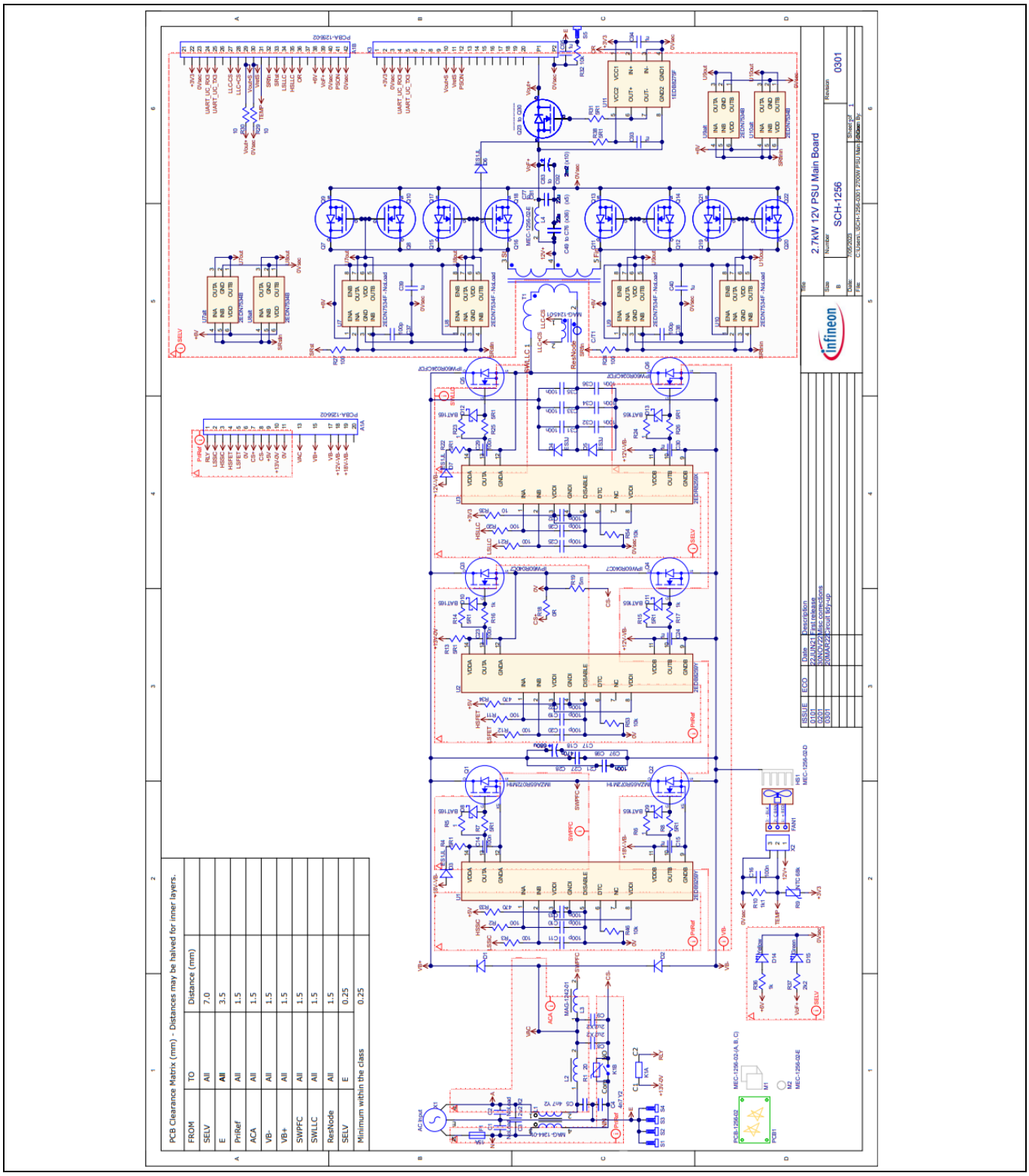

Figure 40 Main board schematic

7.2 Controller board schematic

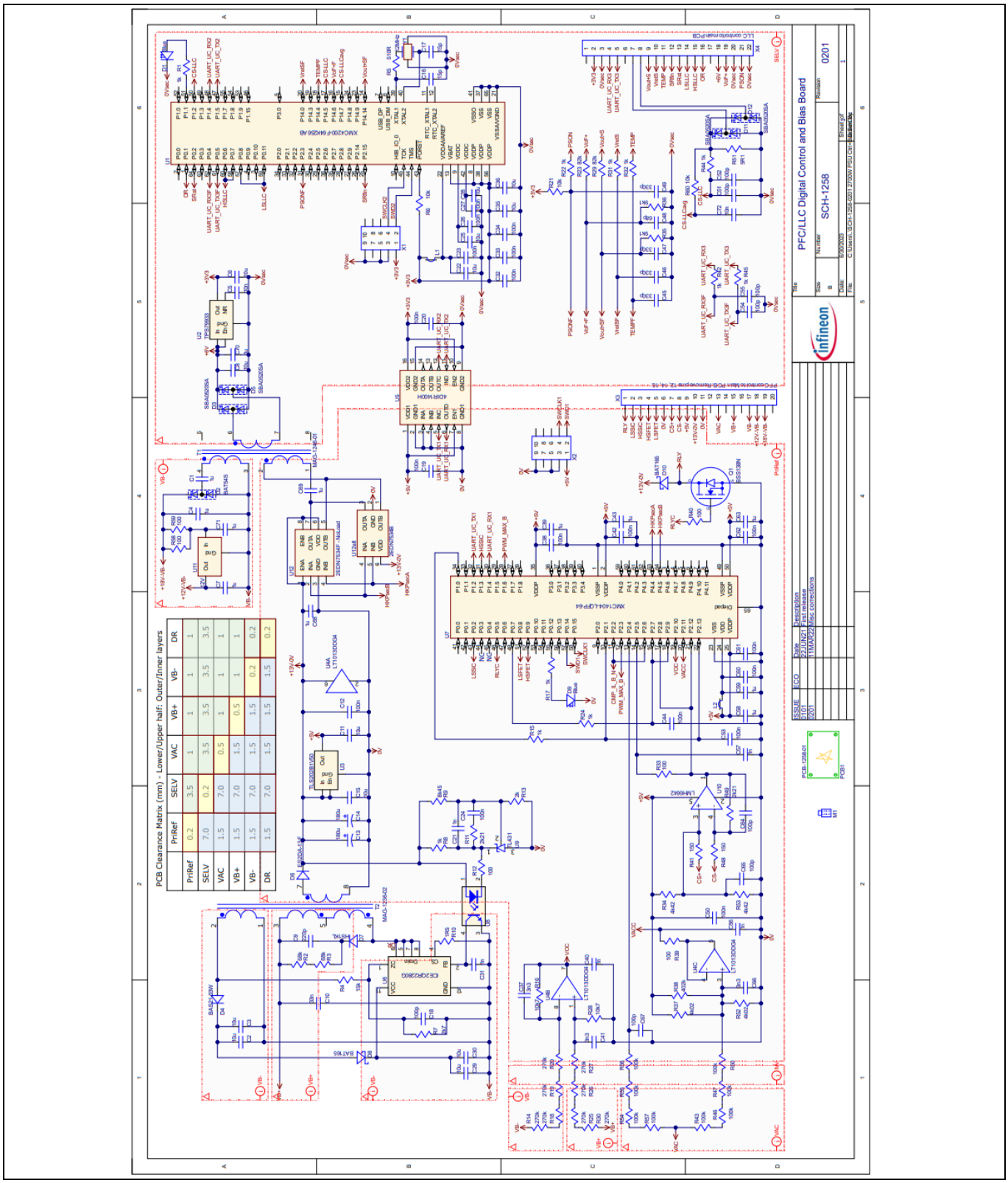

Figure 41 Controller board schematic

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Revision history

Document revision	Date	Description of changes
V 1.0	2023-11-02	Initial release

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